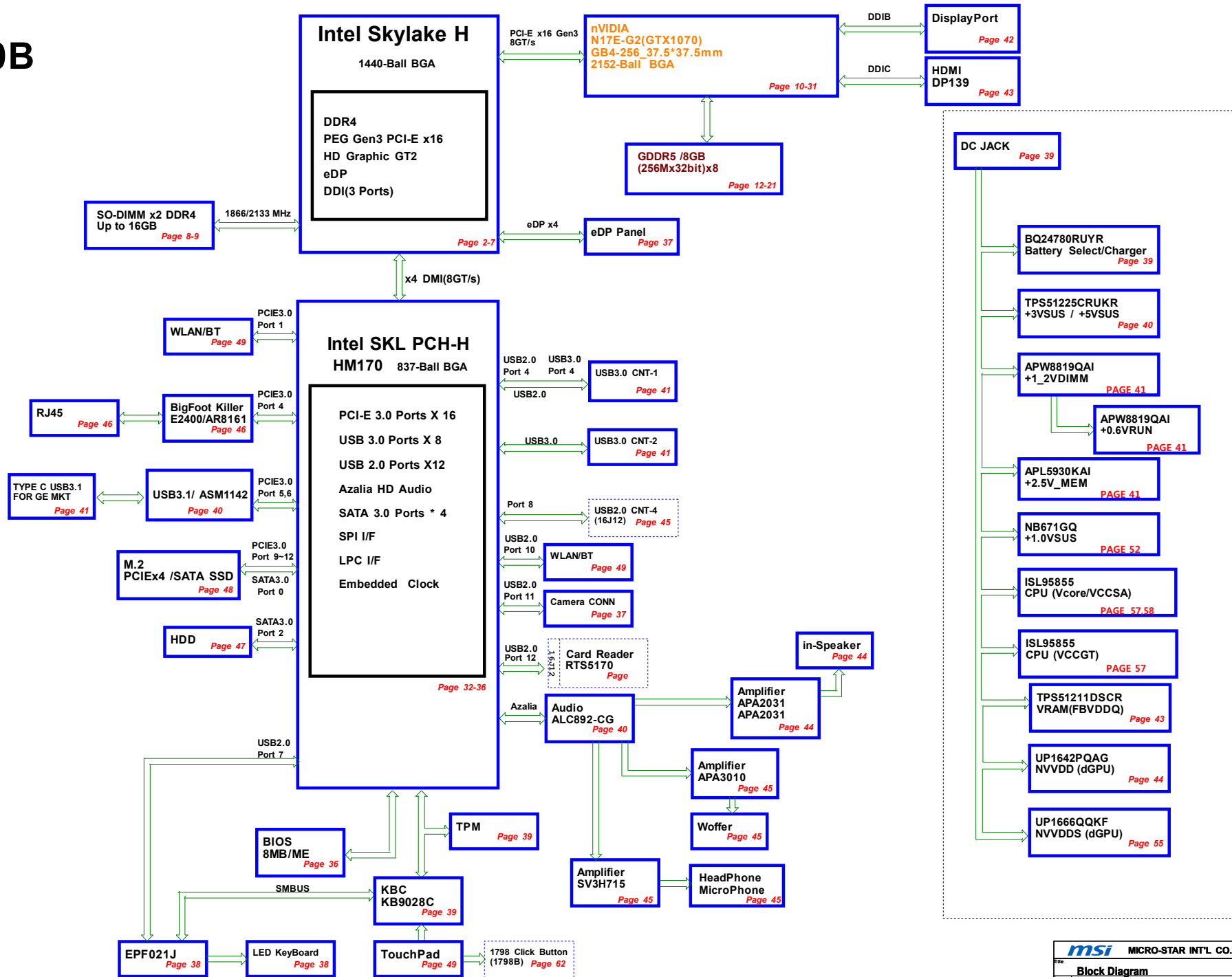
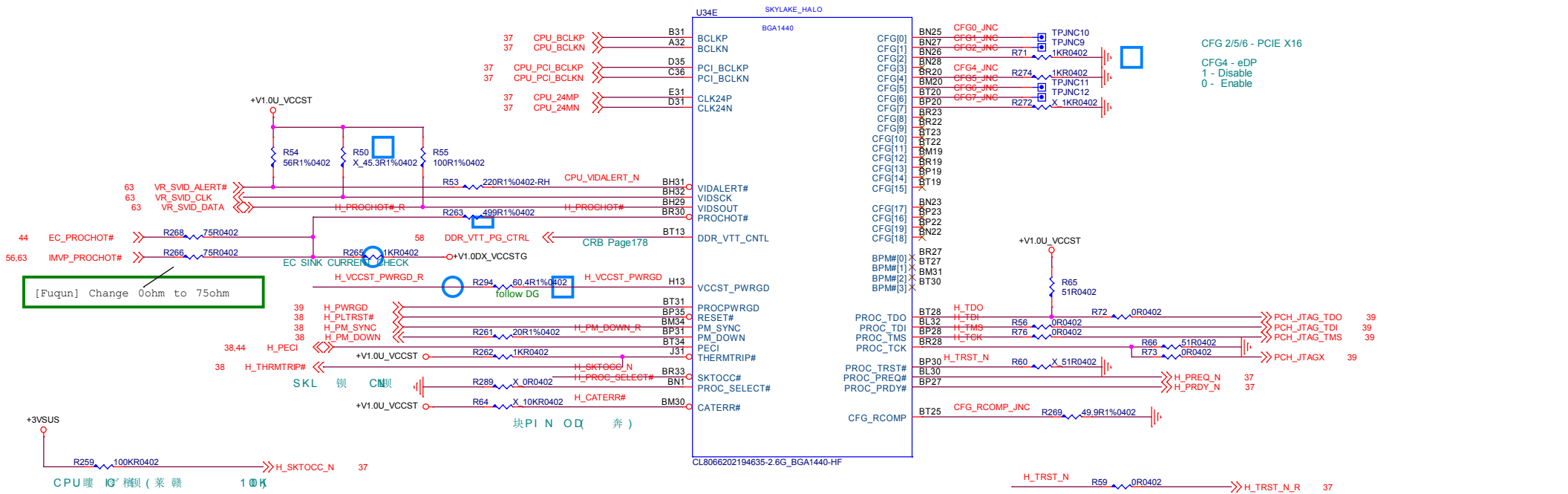


Ver:0B





MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

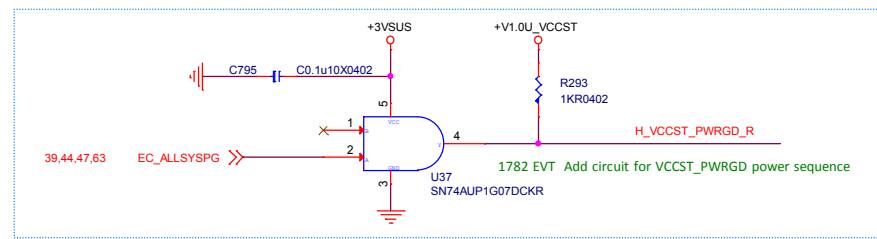
eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

PCI Express * Static X16 Lane Numbering Reversal	
CFG2	CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*

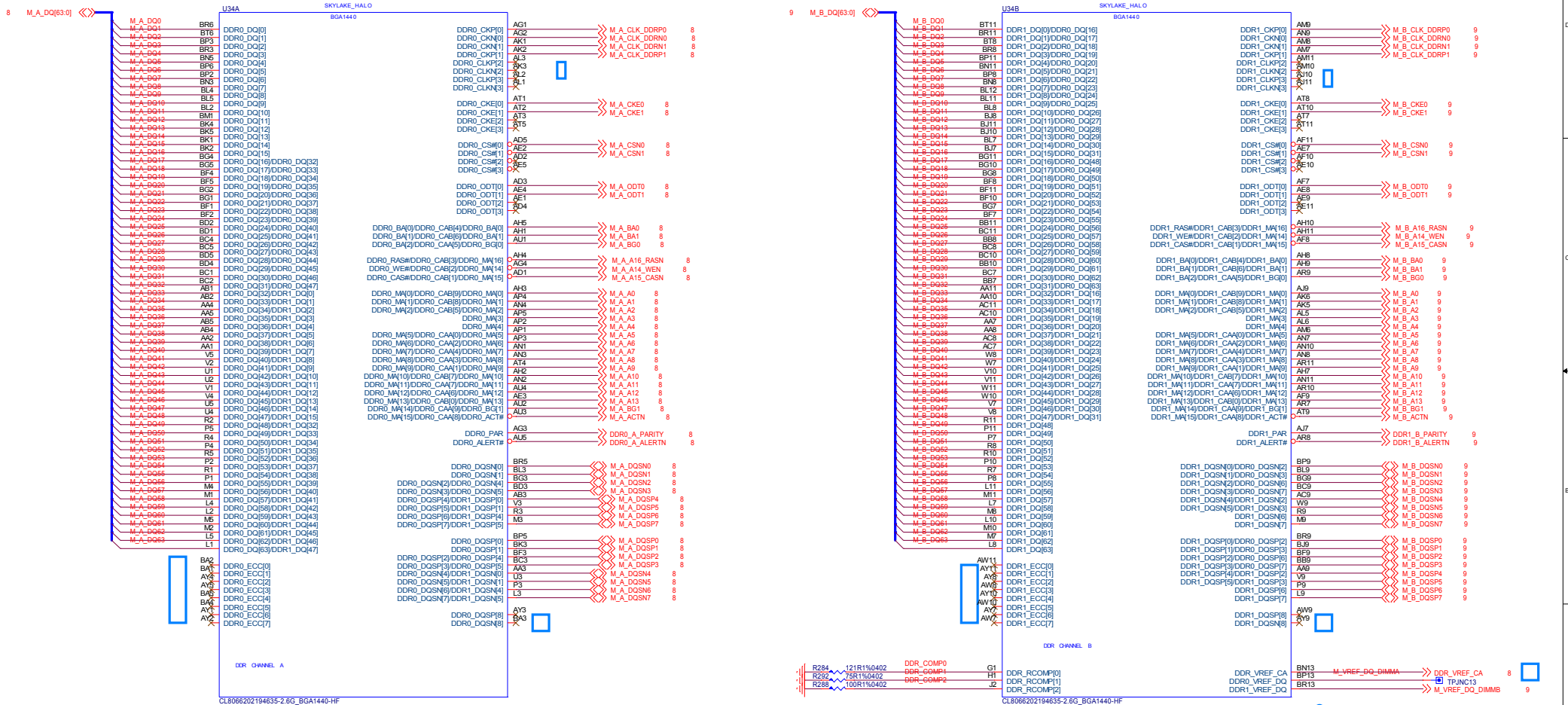
Intel 54492 Page 37,121



CFG 2/5/6 - PCIE X16
CFG4 - eDP
1 - Disable
0 - Enable

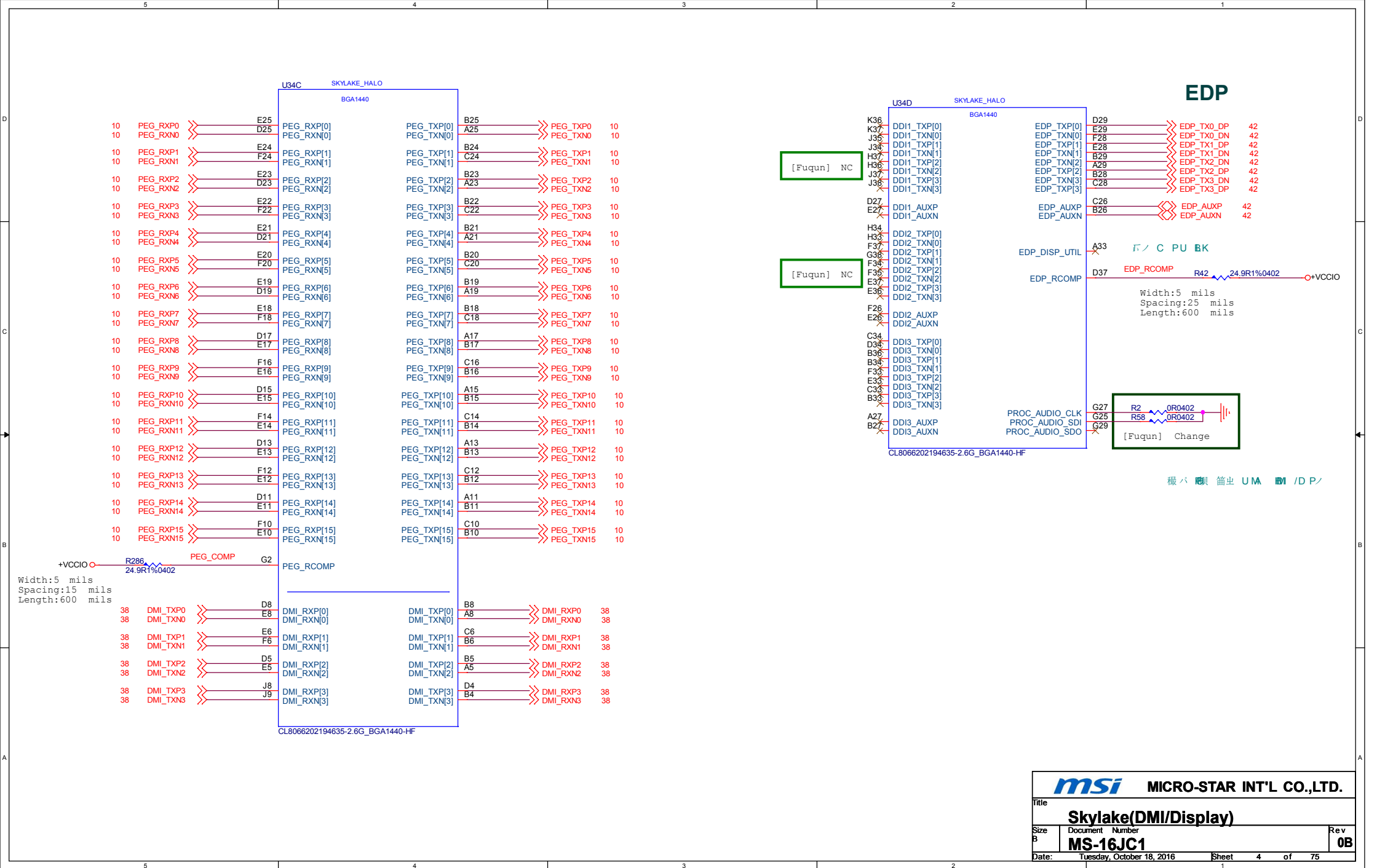
DDR Channel A

DDR Channel B



DG Page 157

msi MICRO-STAR INT'L CO.,LTD.		
Title	Skylake(DDR4)	
Size	Document Number	Rev
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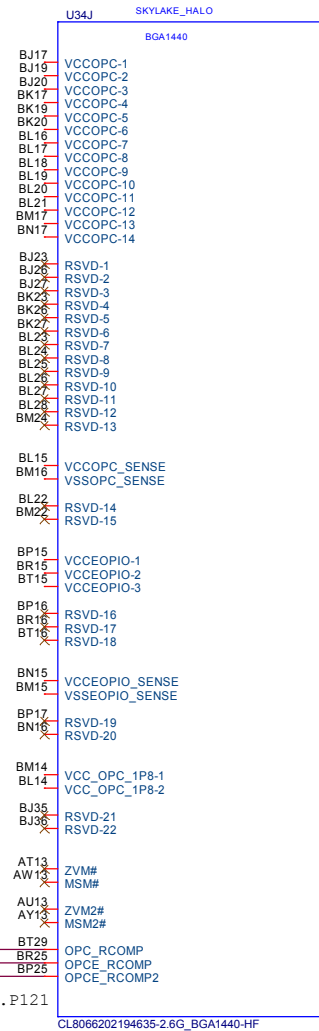


Vinafix.com

GT4 Power

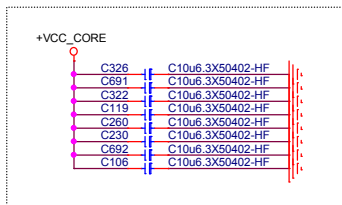
GT4 Power

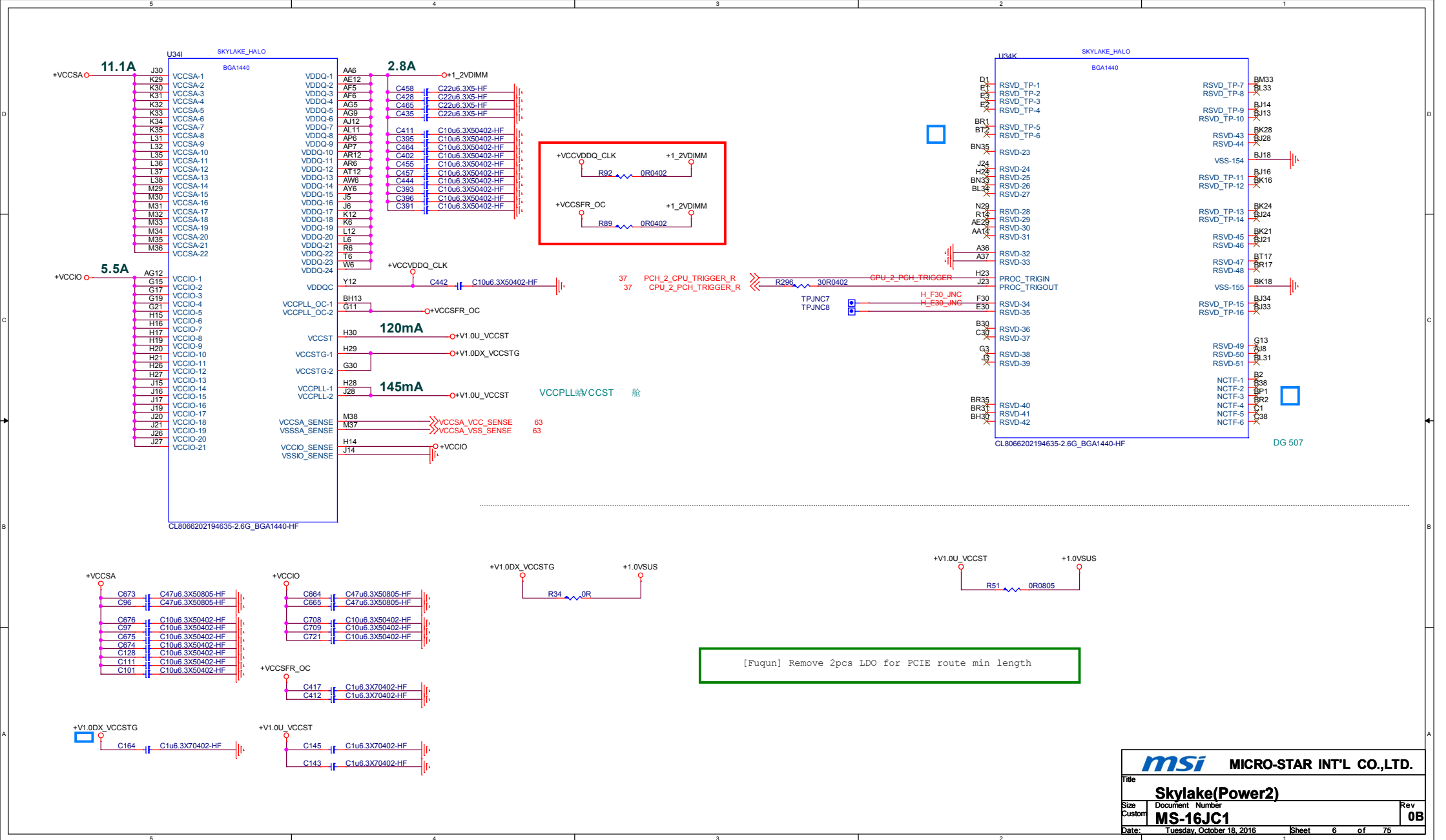
GT4 Power



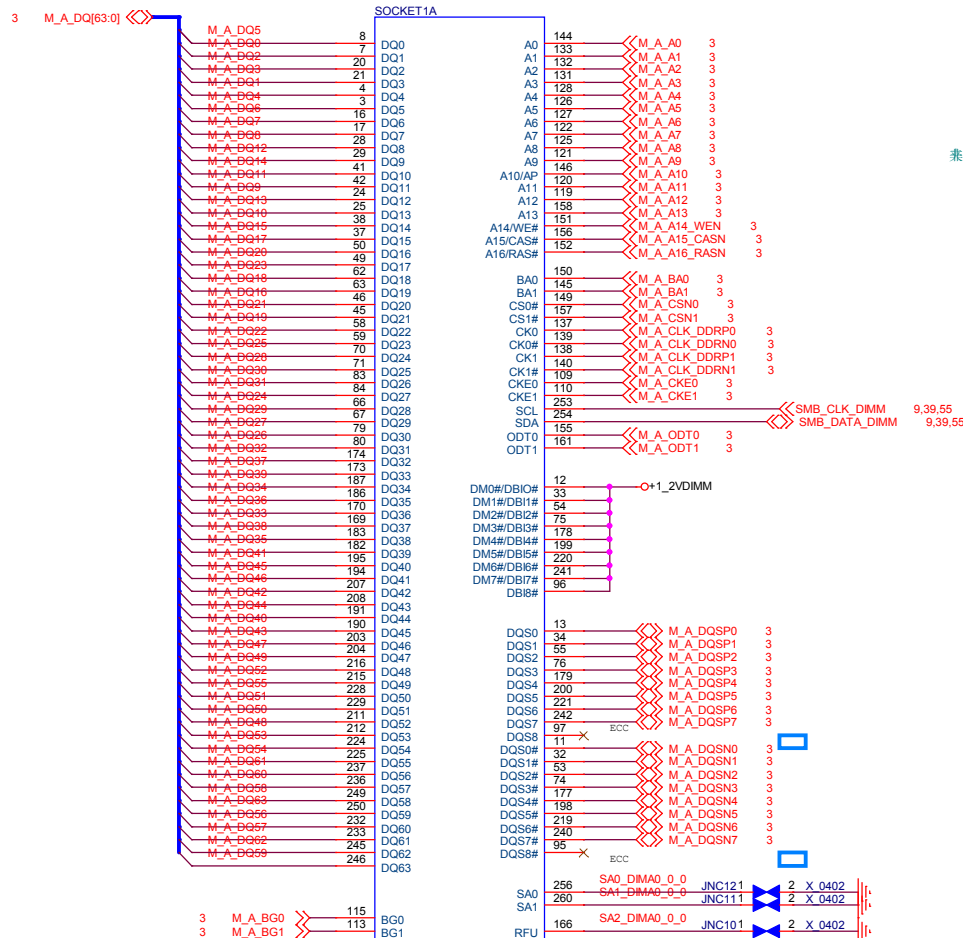
Unconnected for Processors without OPC. EDS.P121

VCCGTx, VCCOPC, VCCOPC_lp8, VCCOEPIO is only applicable to SKUs with OPC

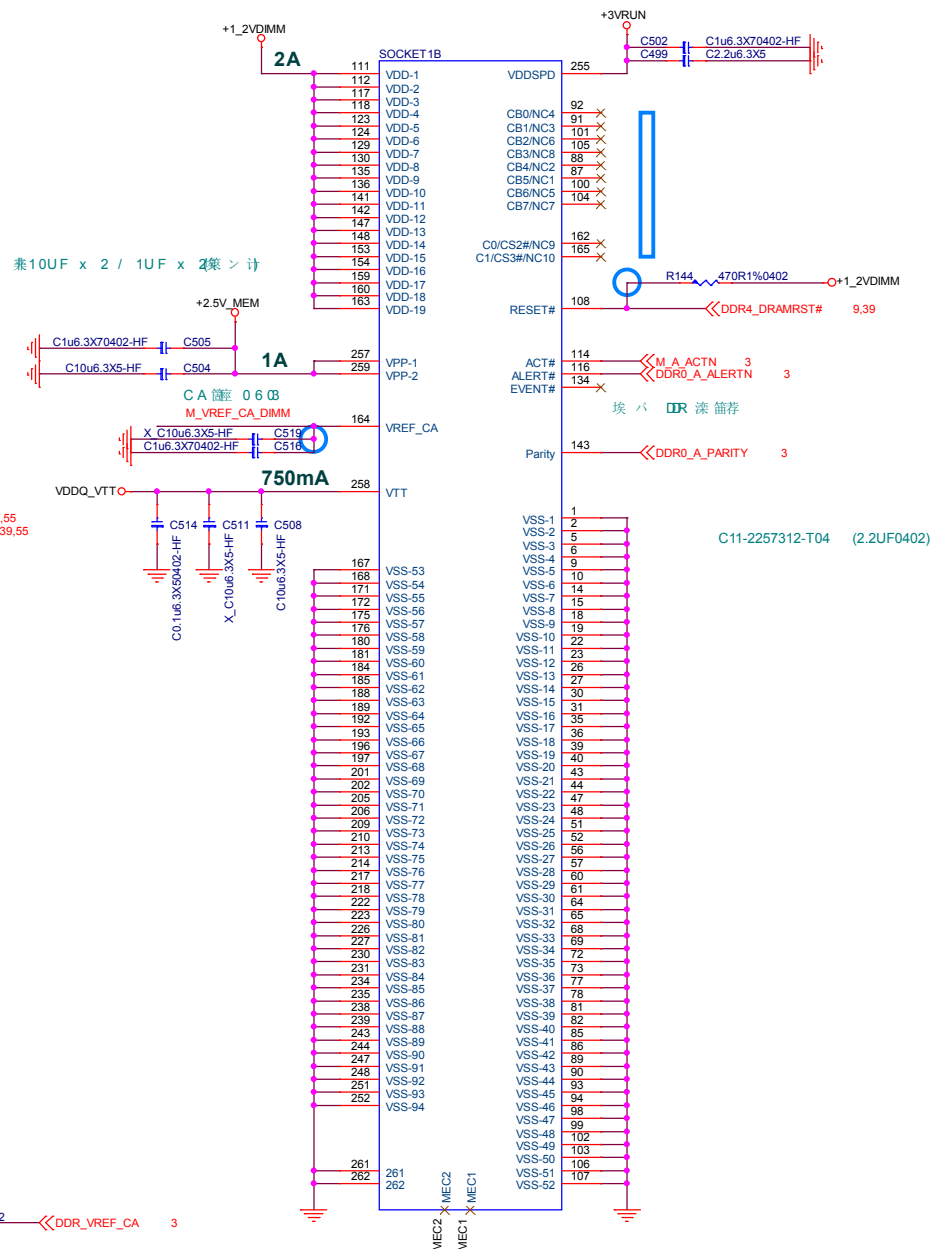
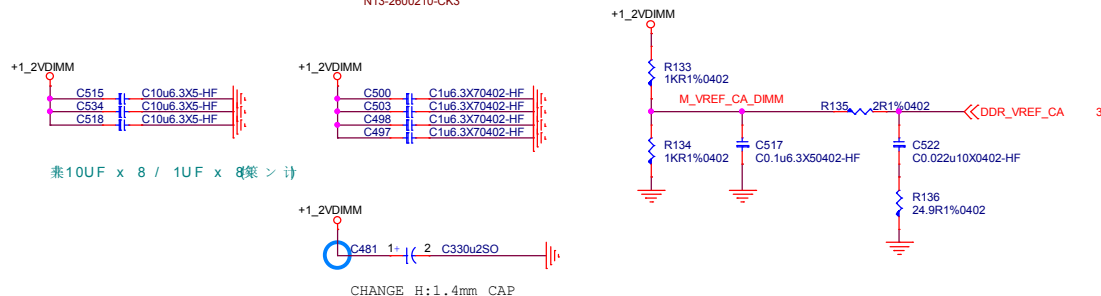





SODIMM_A0 (BOT-Reverse)



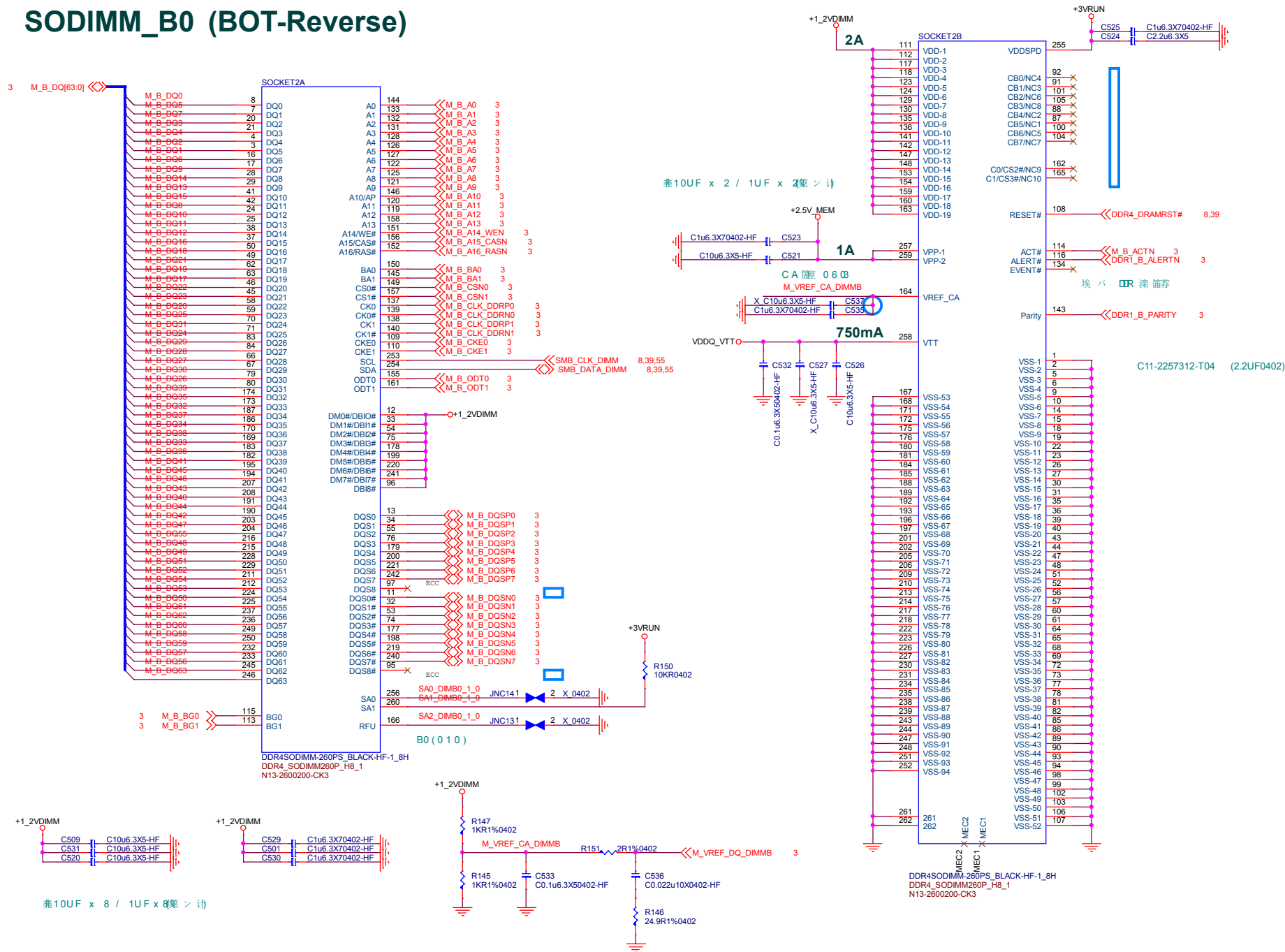
DDR4SODIMM-260PS_BLACK-HF-1_4H
DDR4_SODIMM260P_H4_1
N13-2600210-CK3

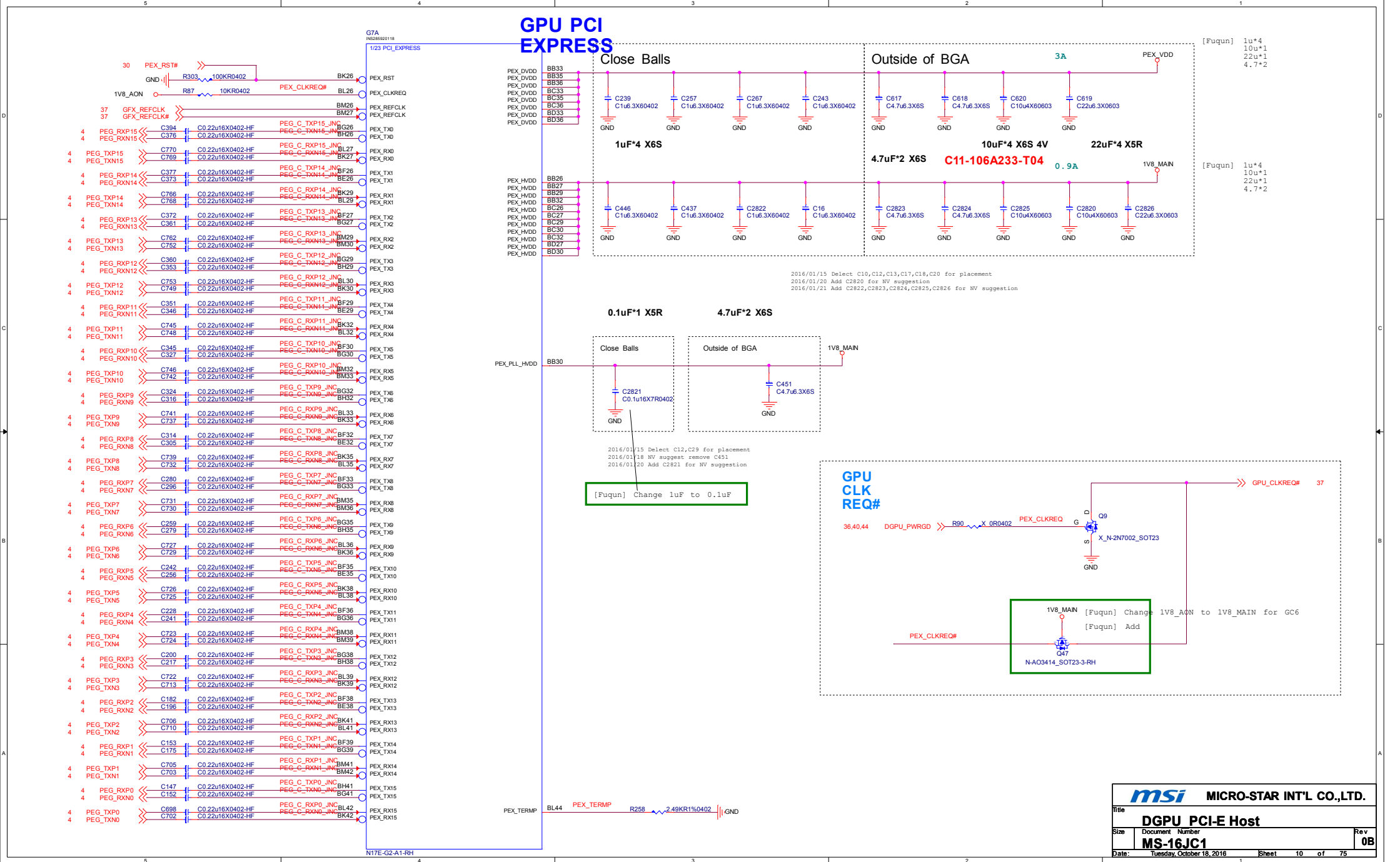


DDR4SODIMM-260PS_BLACK-HF-1_4H
DDR4_SODIMM260P_H4_1
N13-2600210-CK3

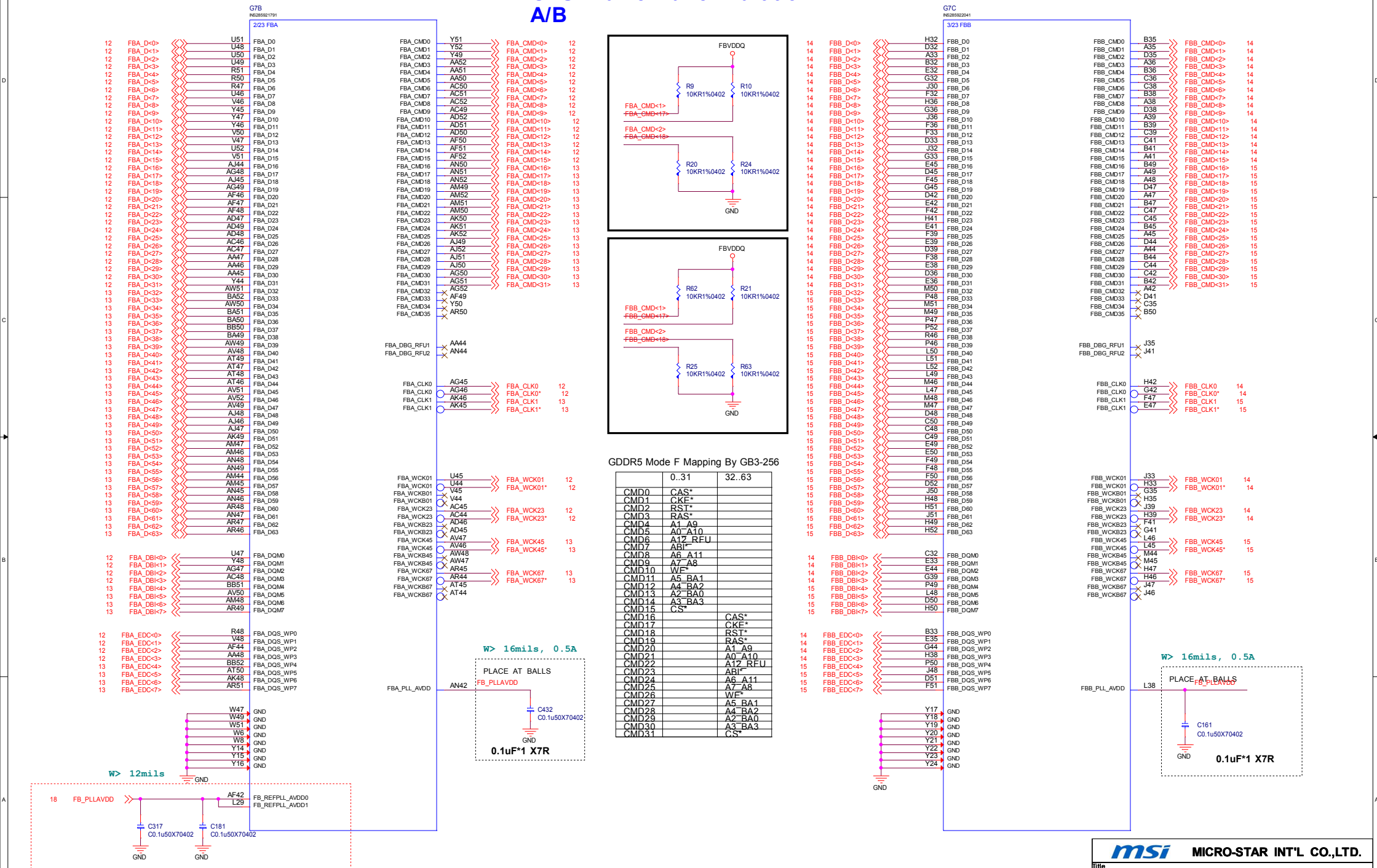
 MICRO-STAR INT'L CO.,LTD.	
Title: DDR4 SODIMM_A0	
Size Customer:	Document Number MS-16JC1
Date:	Rev 0B
Tuesday, October 18, 2016 Sheet 8 of 75	

SODIMM_B0 (BOT-Reverse)

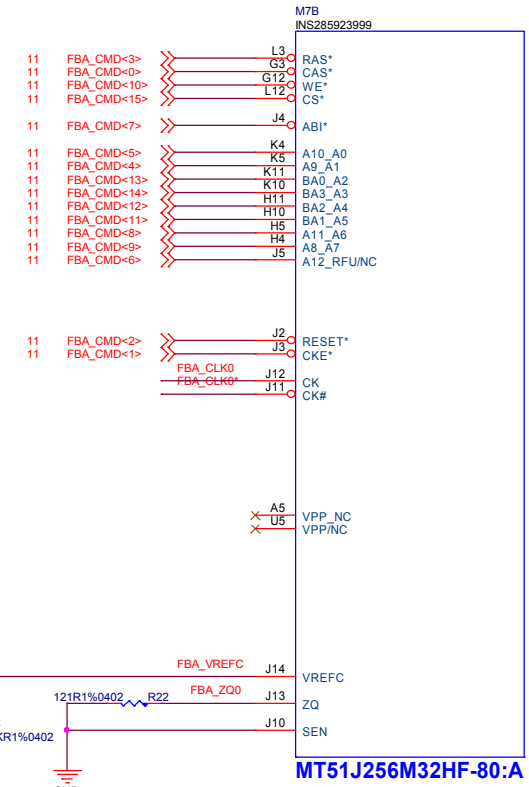
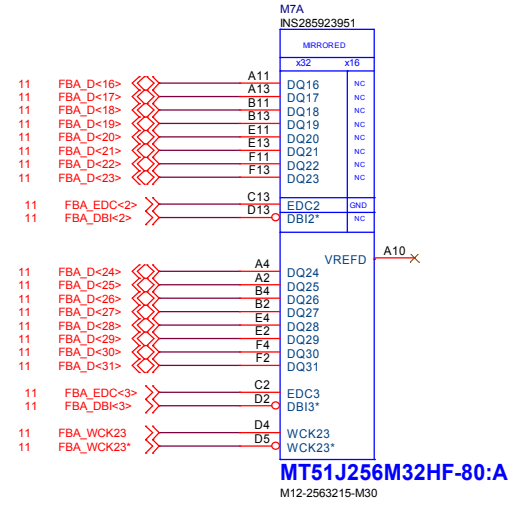




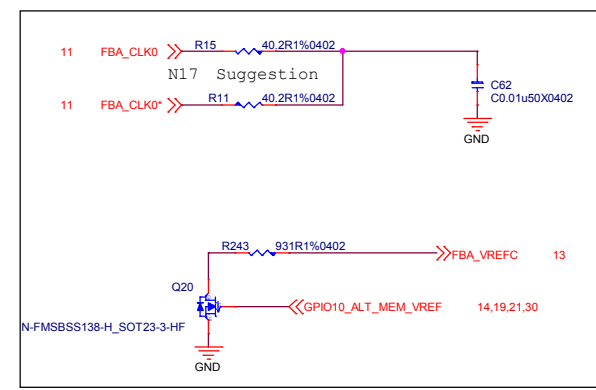
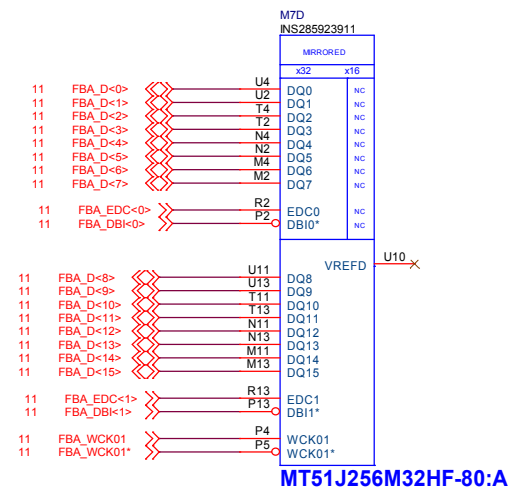
GPU Frame Buffer Partition A/B



DGPU_GDDR5 FrameBuffer A0



[Fuqun] R245 footprint C0402_MXM_1 ?



msi MICRO-STAR INT'L CO.,LTD.

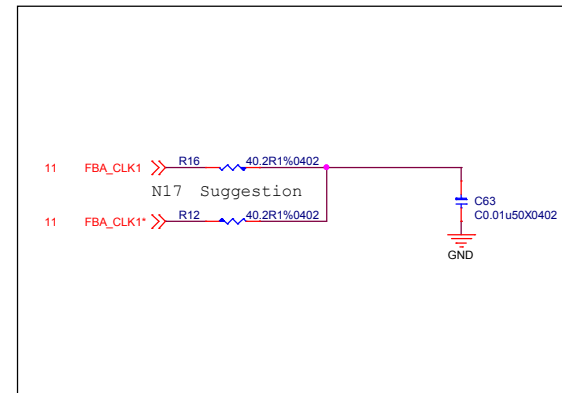
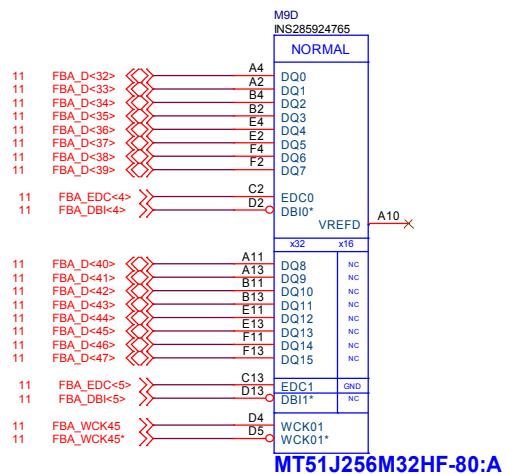
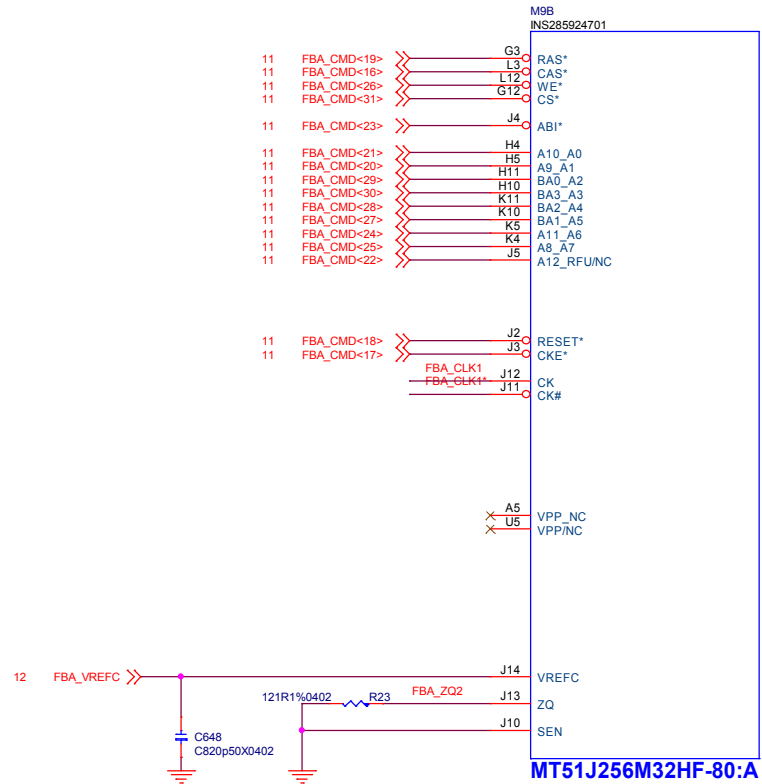
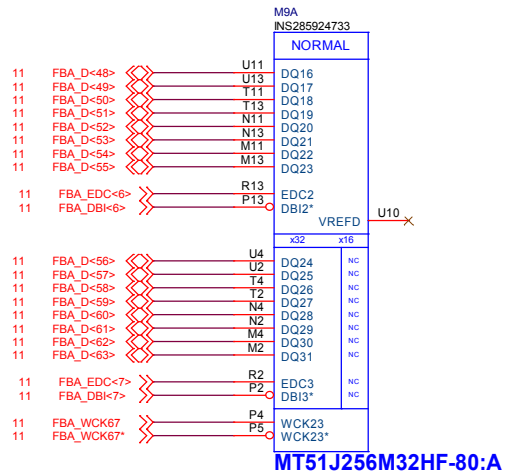
Title **DGPU_GDDR5 FrameBuffer A0**

Size Document Number **MS-16JC1** Rev **0B**

Date: Tuesday, October 18, 2016 Sheet 12 of 75

Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)
Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

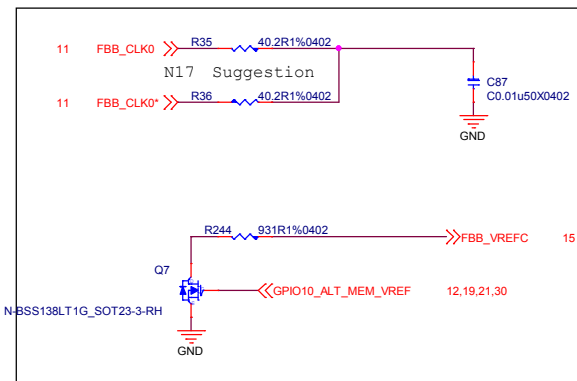
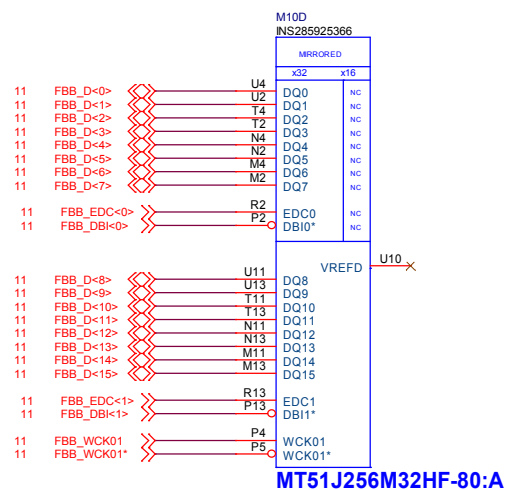
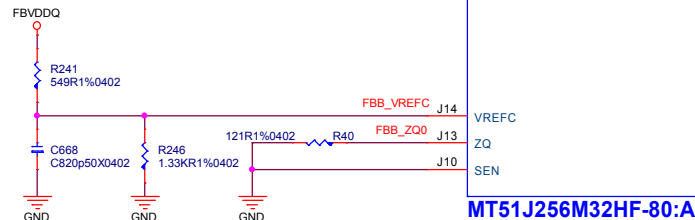
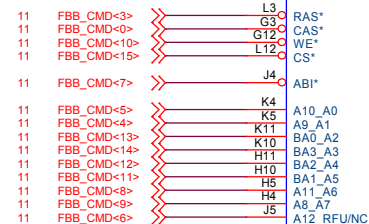
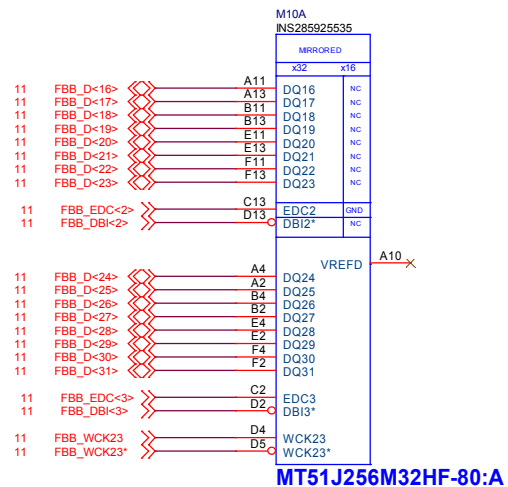
DGPU_GDDR5 FrameBuffer A1



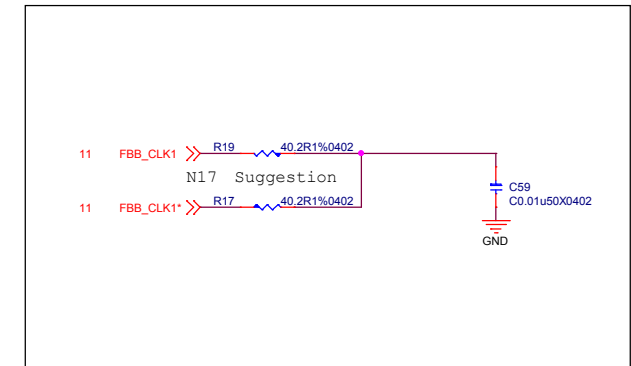
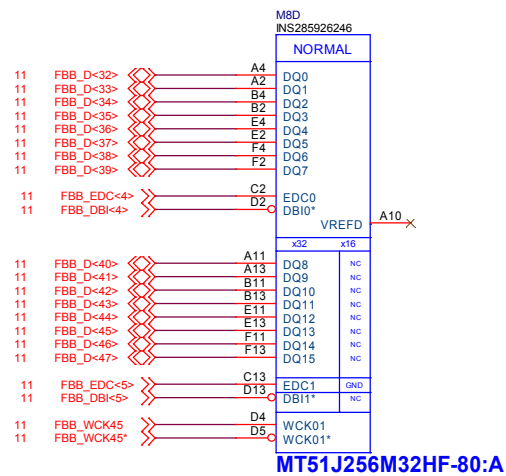
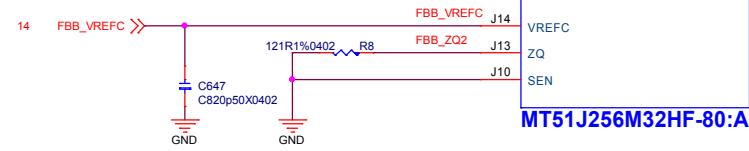
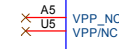
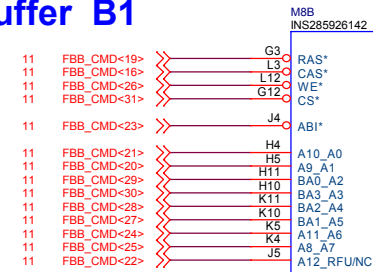
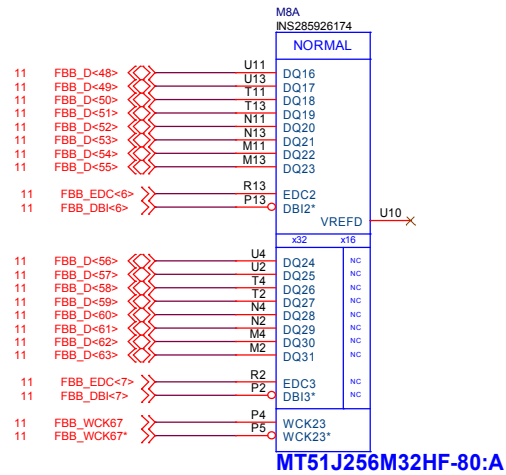
msi MICRO-STAR INT'L CO.,LTD.	
Title DGPU GDDR5 FrameBuffer A1	
Size	Document Number MS-16JC1
Date:	Tuesday, October 18, 2016
Sheet	13 of 75
Rev	0B

Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)
Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

DGPU_GDDR5 FrameBuffer B0



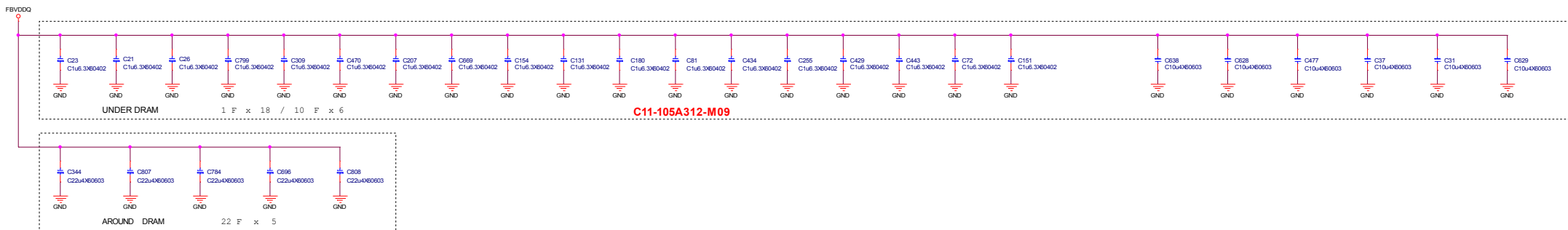
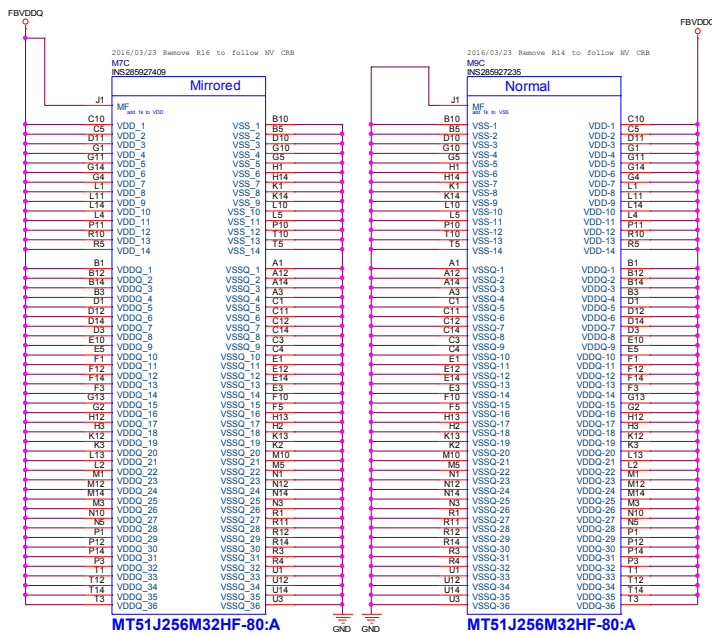
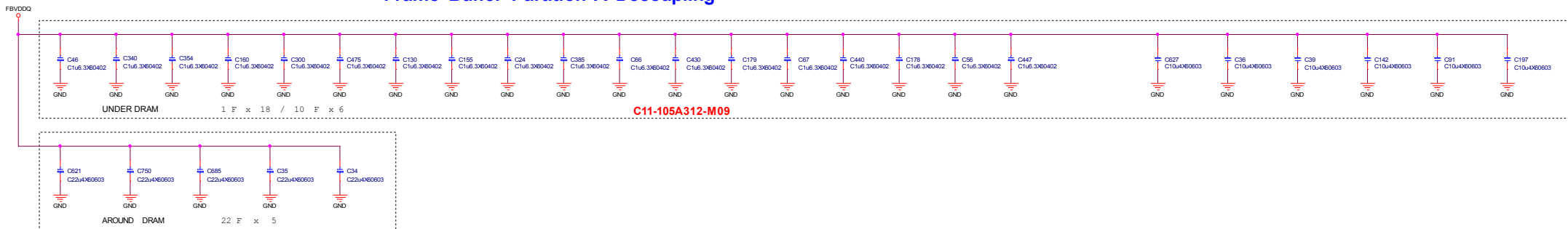
DGPU_GDDR5 FrameBuffer B1



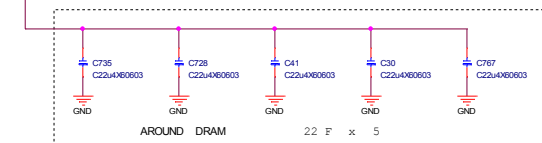
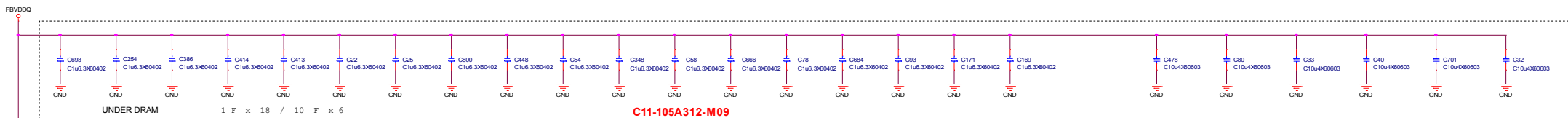
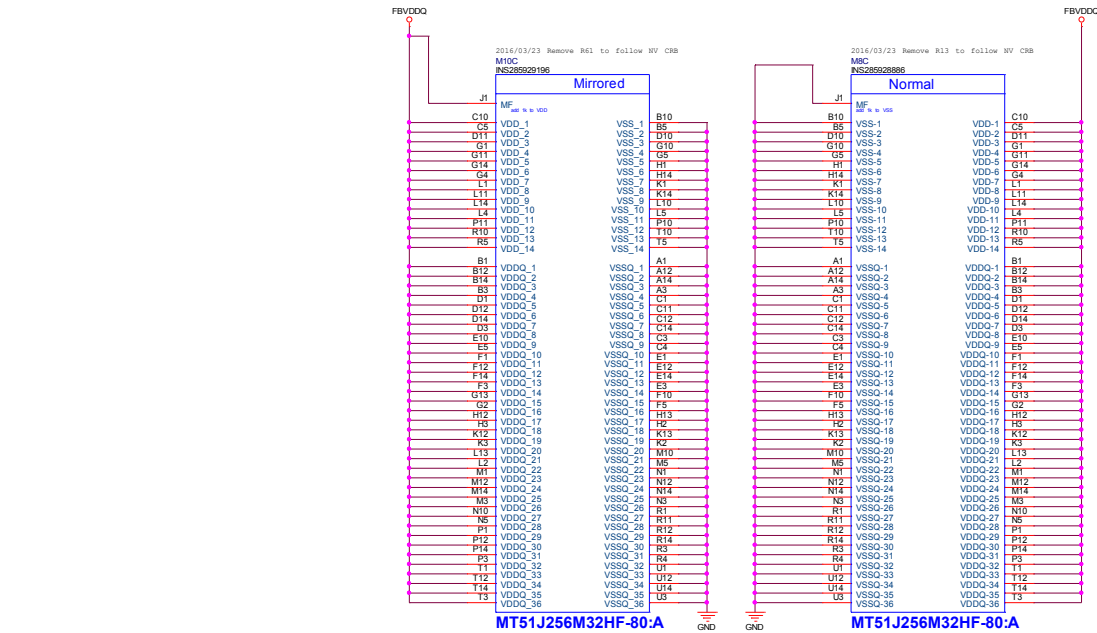
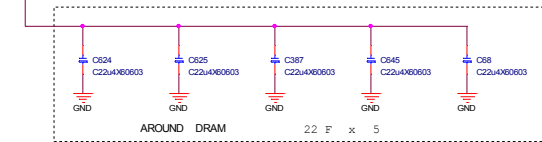
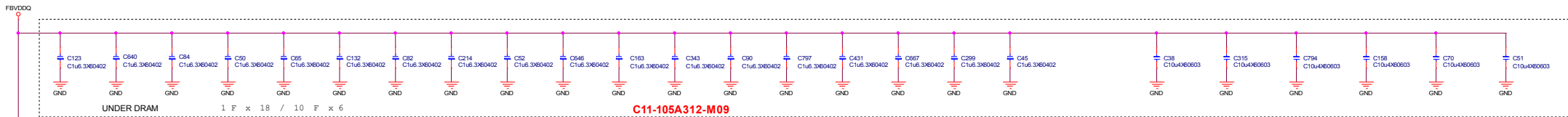
Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)
Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

msi MICRO-STAR INT'L CO.,LTD.			
Title DGPU GDDR5 FrameBuffer B1			
Size	Document	Number	Rev
		MS-16JC1	0B
Date:	Tuesday, October 18, 2016		Sheet 15 of 75

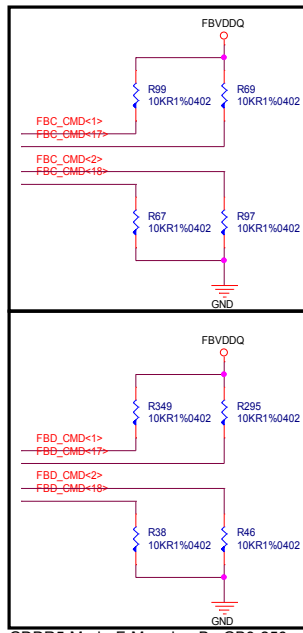
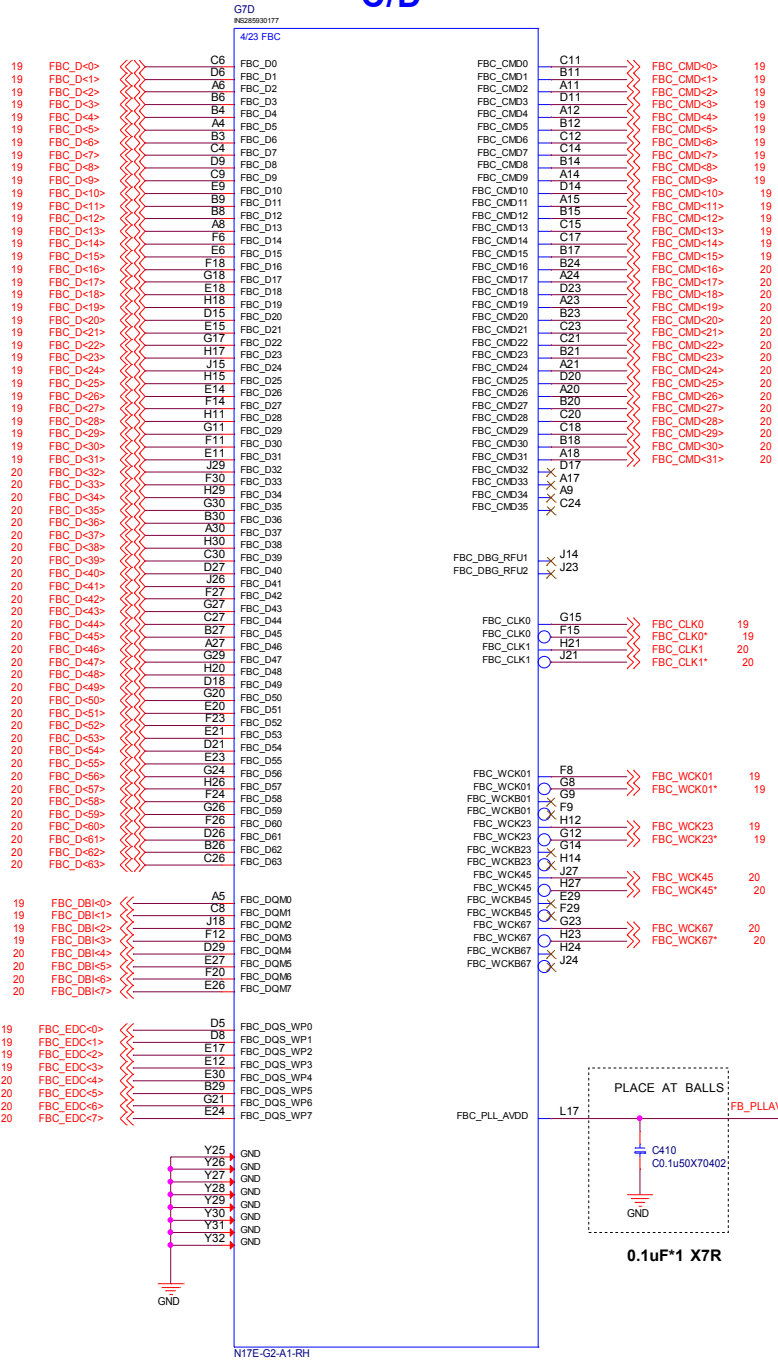
Frame Buffer Partition A Decoupling



Frame Buffer Partition B Decoupling

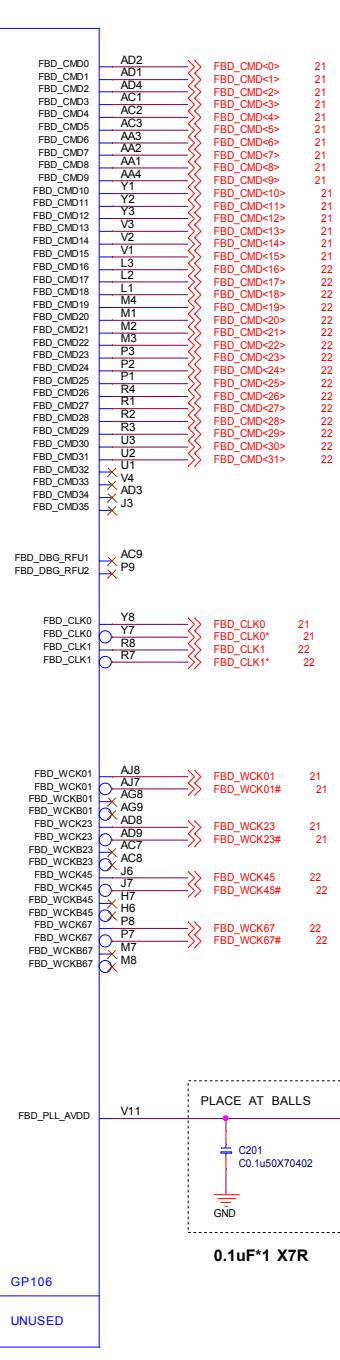
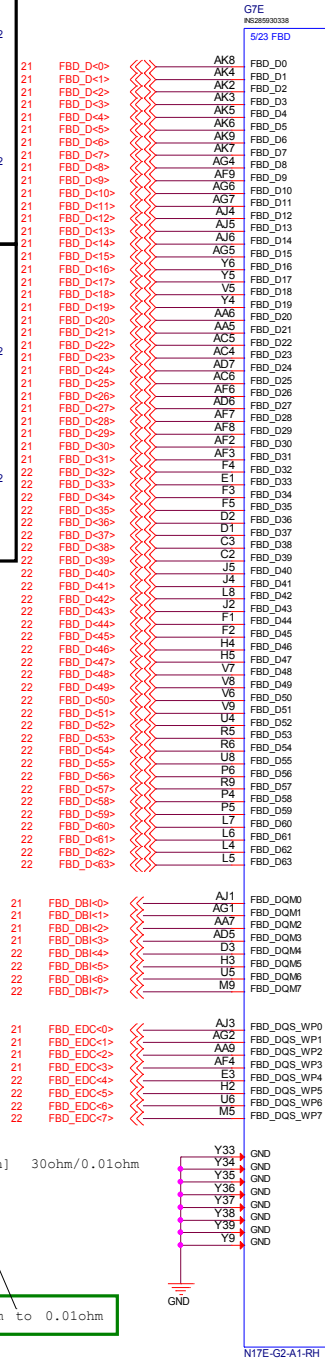


GPU Frame Buffer Partition C/D



GDDR5 Mode F Mapping By GB3-256

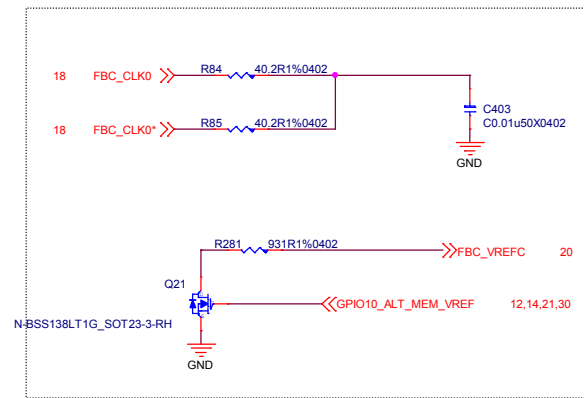
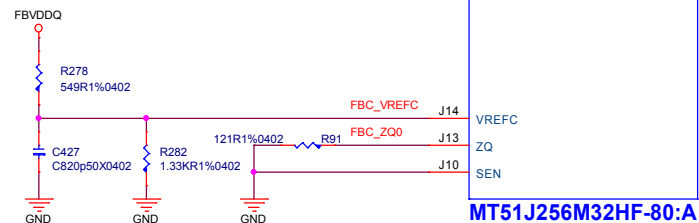
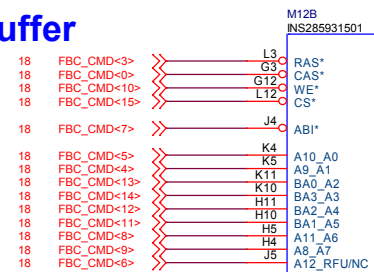
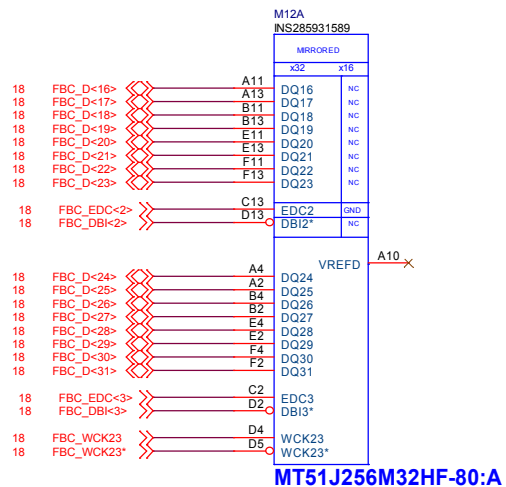
	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1 A9	
CMD5	A0 A10	
CMD6	A12 RFU	
CMD7	AB1*	
CMD8	A6 A11	
CMD9	A7 A8	
CMD10	WE*	
CMD11	A5 BA1	
CMD12	A4 BA2	
CMD13	A3 BA3	
CMD14	A3 BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1 A9
CMD21		A0 A10
CMD22		A12 RFU
CMD23		AB1*
CMD24		A6 A11
CMD25		A7 A8
CMD26		WE*
CMD27		A5 BA1
CMD28		A4 BA2
CMD29		A3 BA3
CMD30		A3 BA3
CMD31		CS*



[Fuqun] ESR change 0.03ohm to 0.01ohm

GP104	GP106
FBD	UNUSE

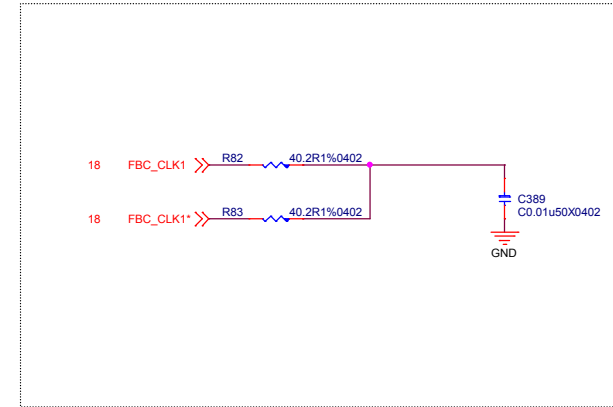
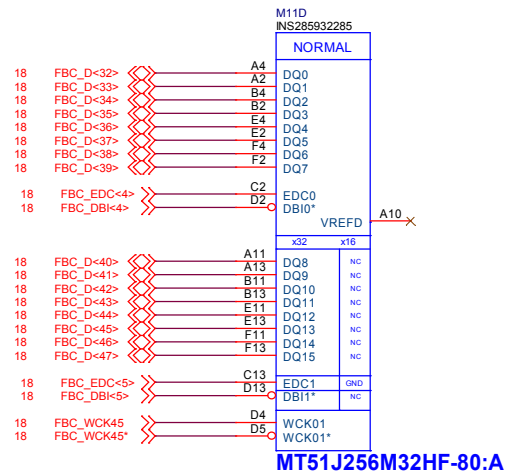
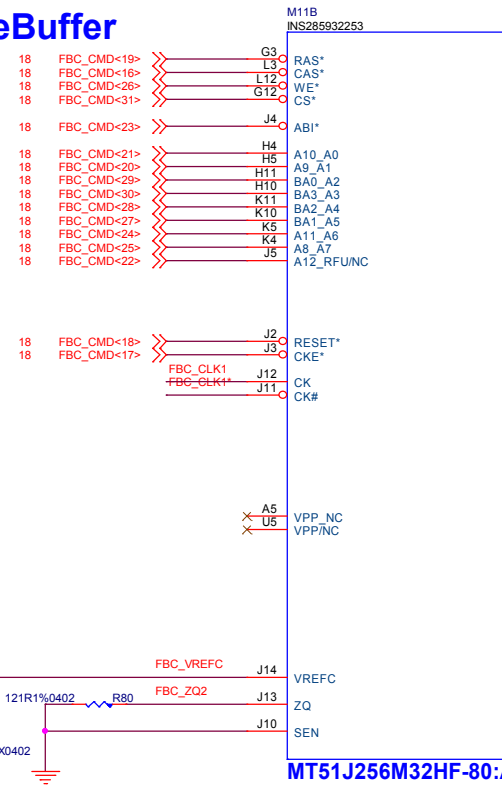
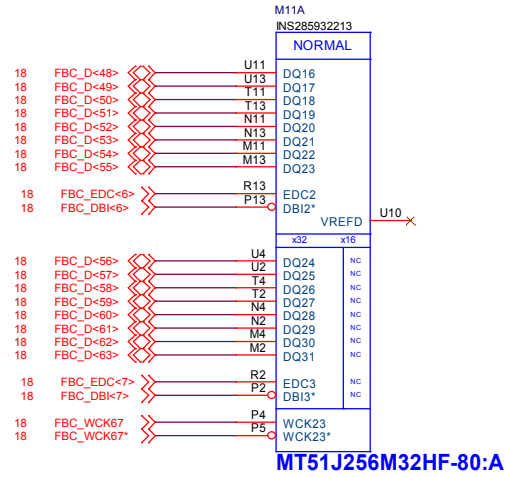
DGPU_GDDR5 FrameBuffer C0



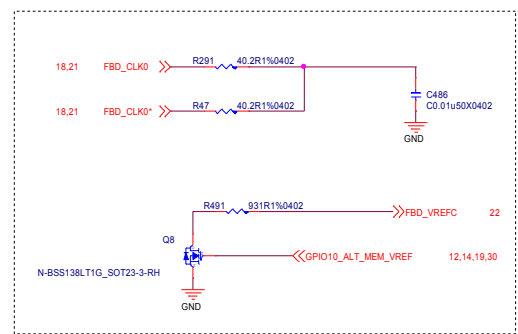
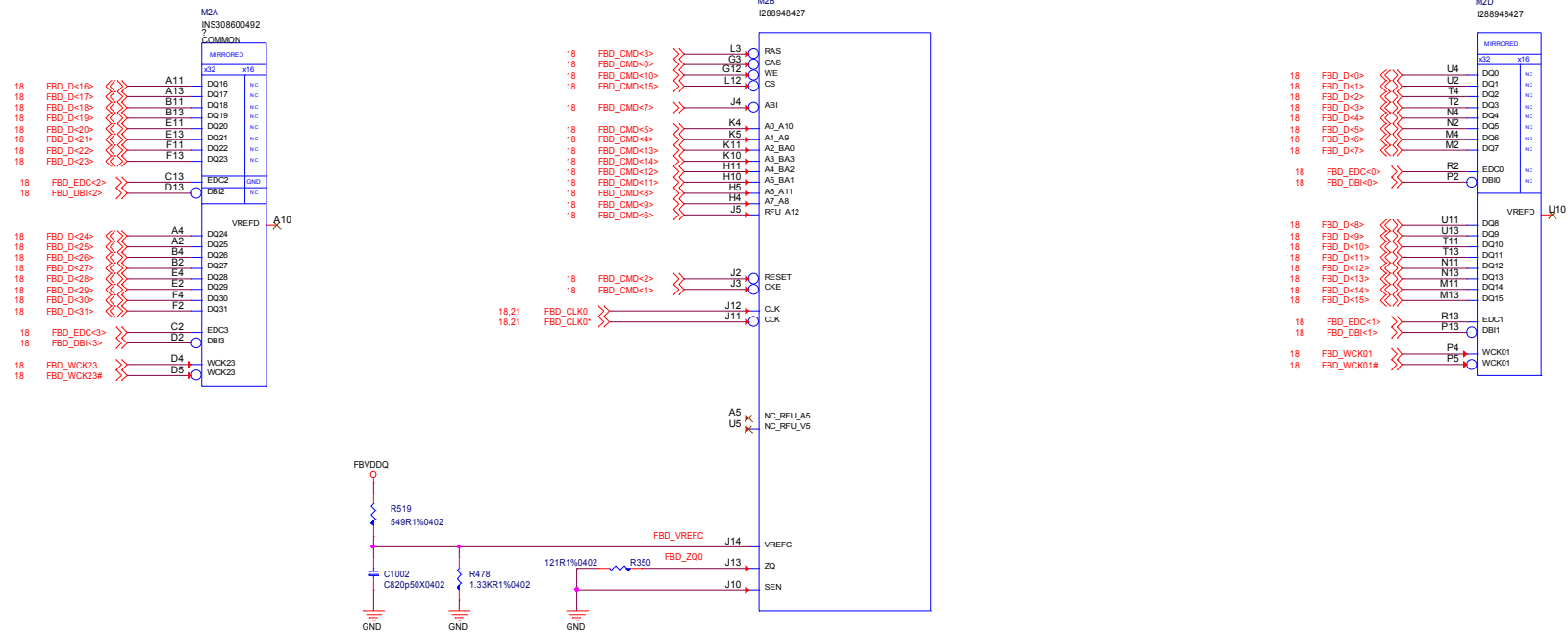
msi MICRO-STAR INT'L CO.,LTD.			
Title DGPU_GDDR5 FrameBuffer C			
Size	Document	Number	Rev
		MS-16JC1	0B
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Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)
Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

DGPU_GDDR5 FrameBuffer C1

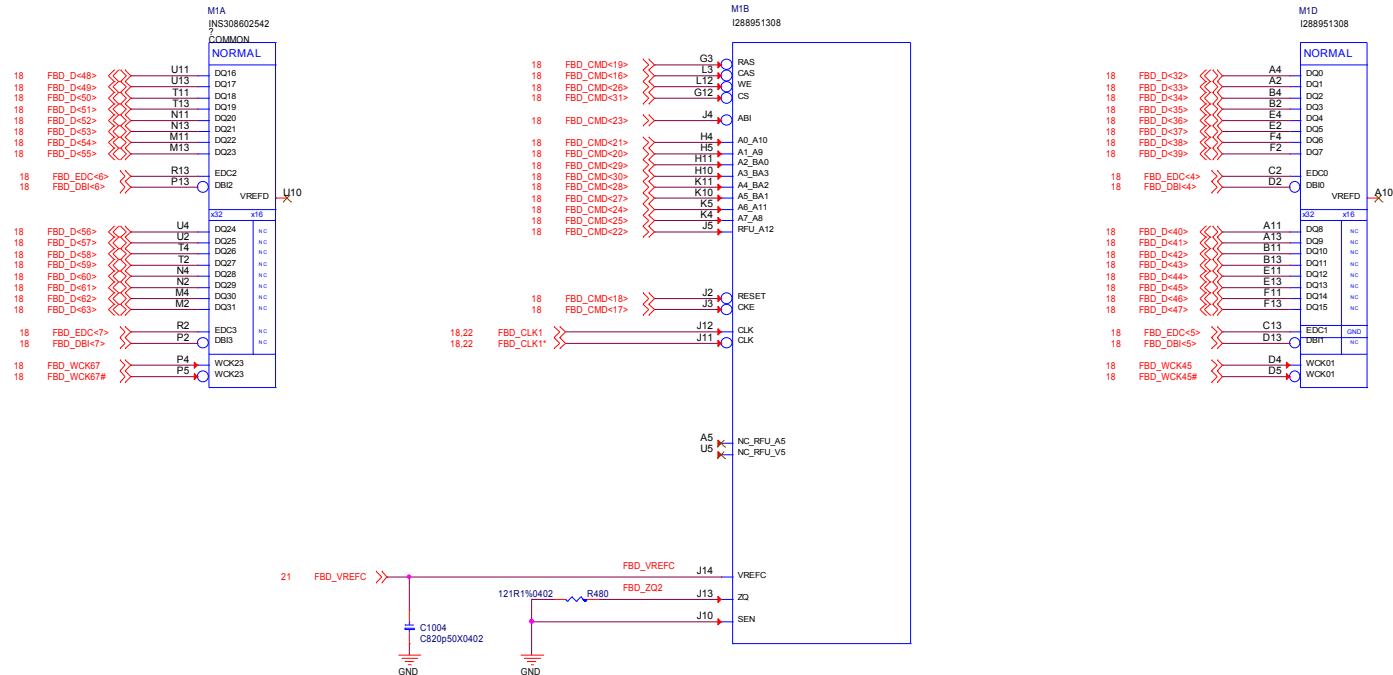


DGPU_GDDR5 FrameBuffer D0

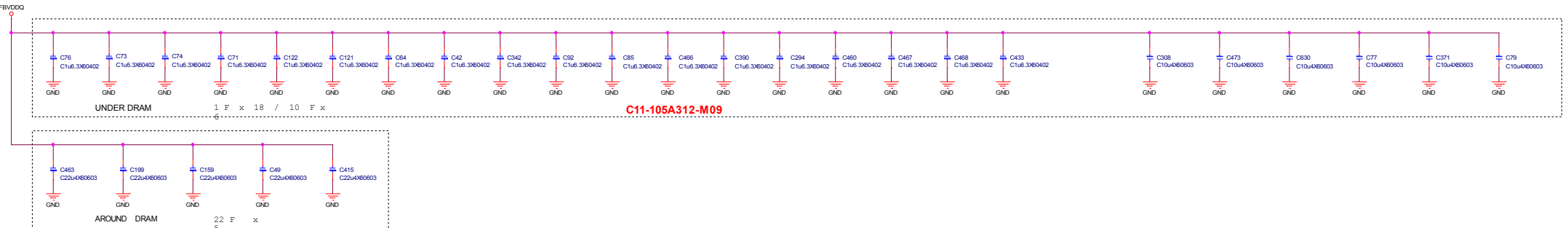
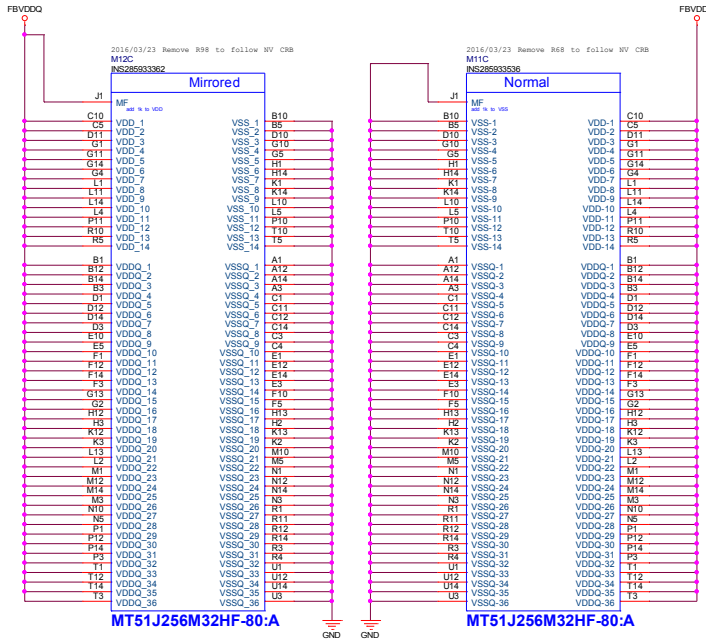
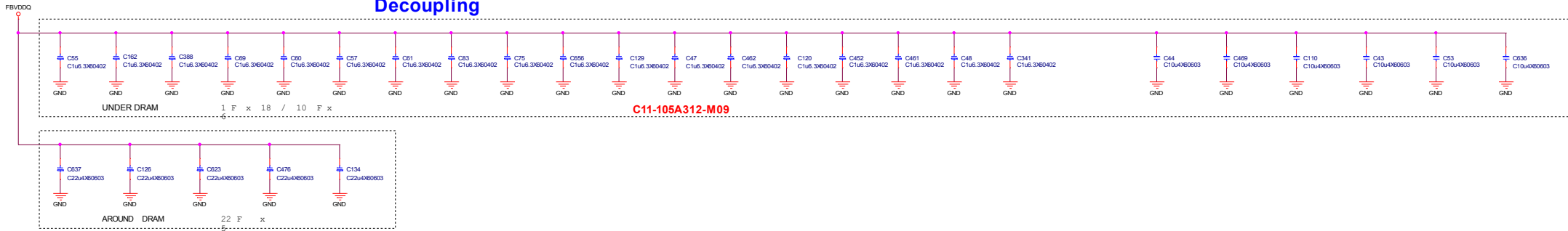


Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)
 Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

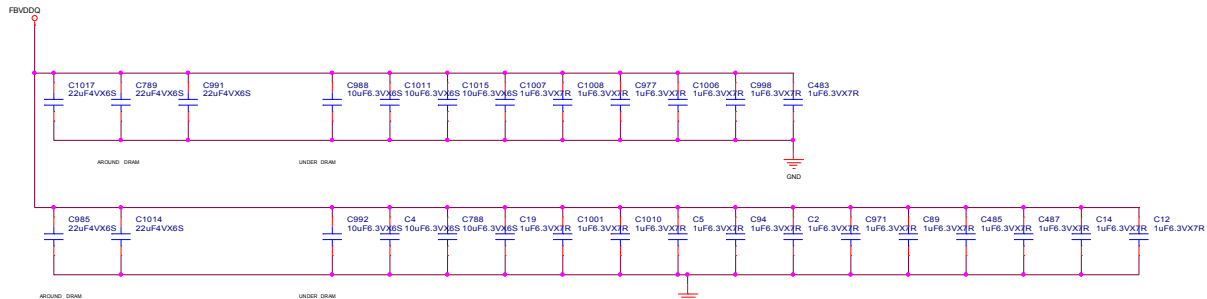
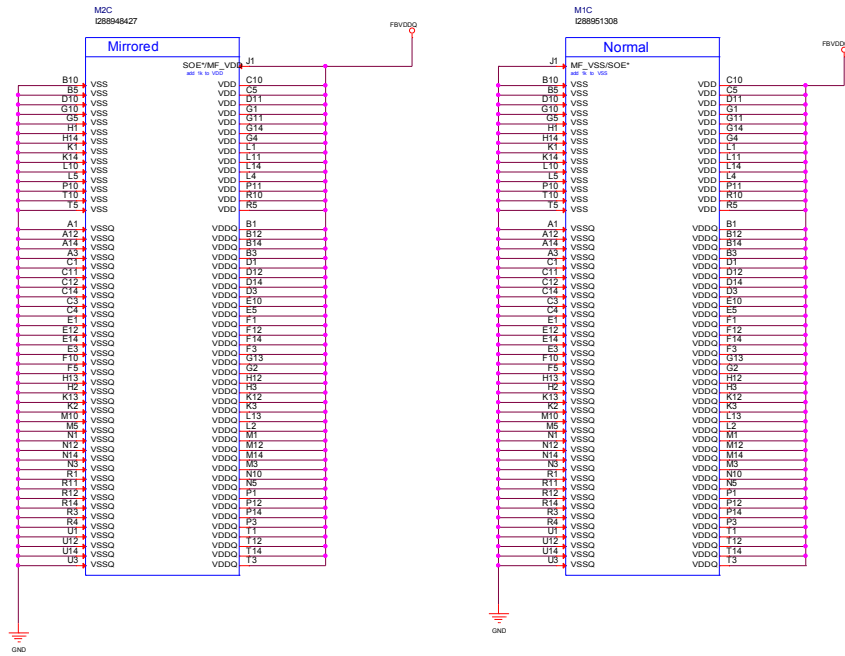
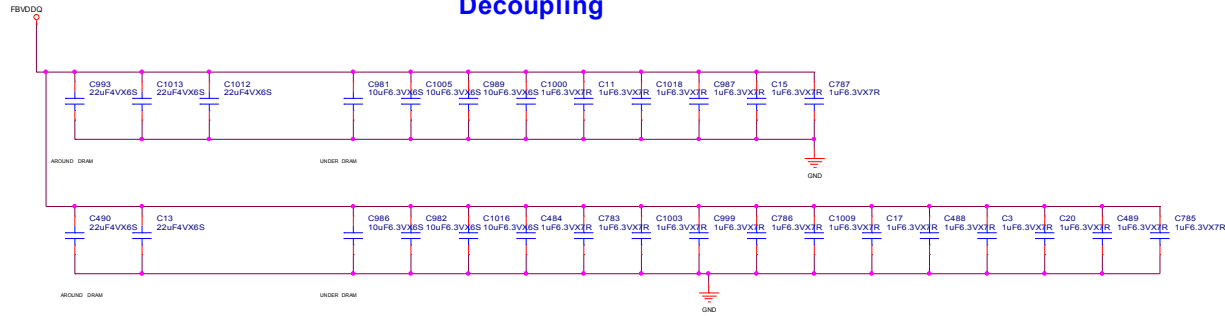
DGPU_GDDR5 FrameBuffer D1



Frame Buffer Partition C Decoupling



Frame Buffer Partition D Decoupling

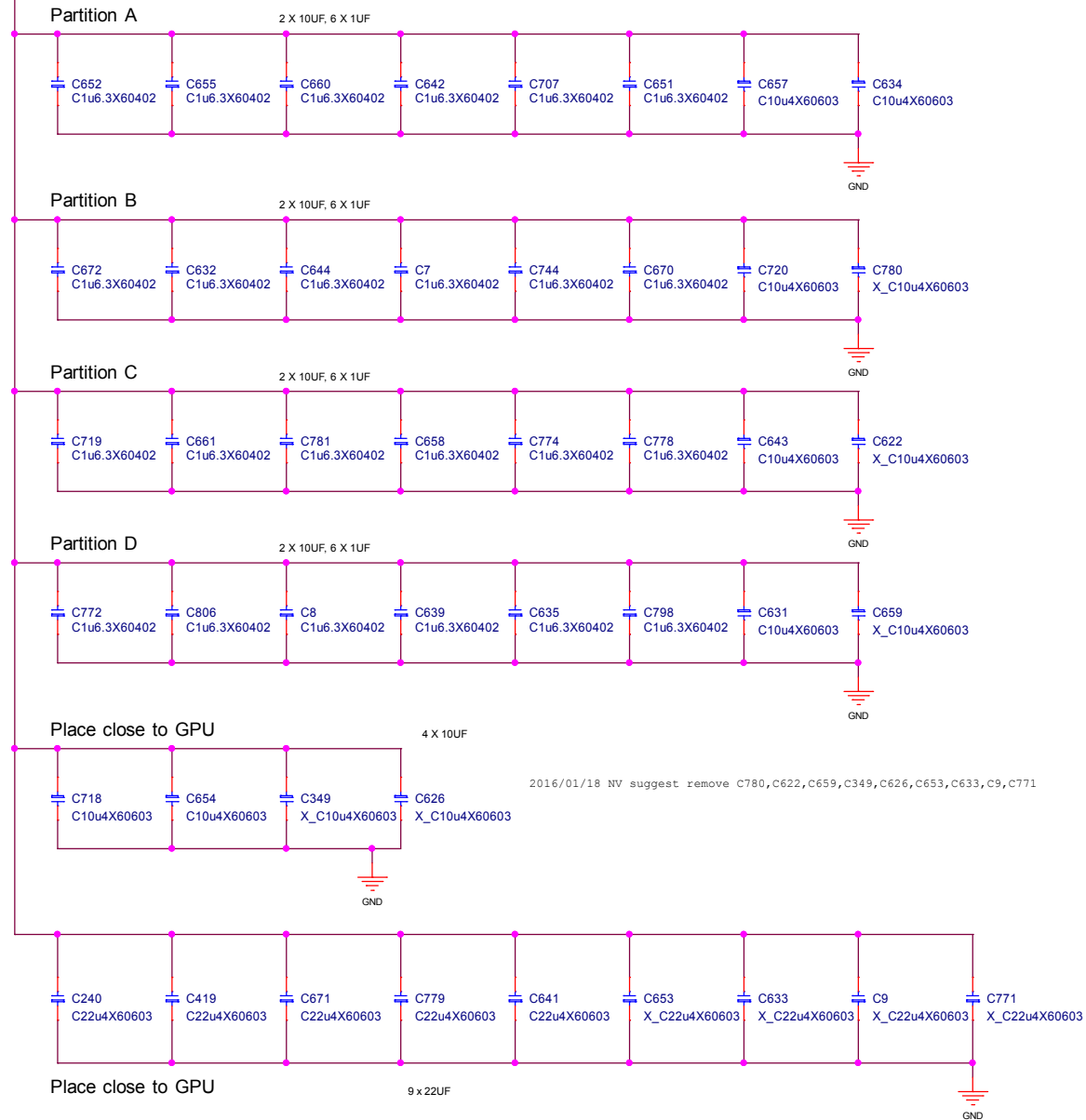



A



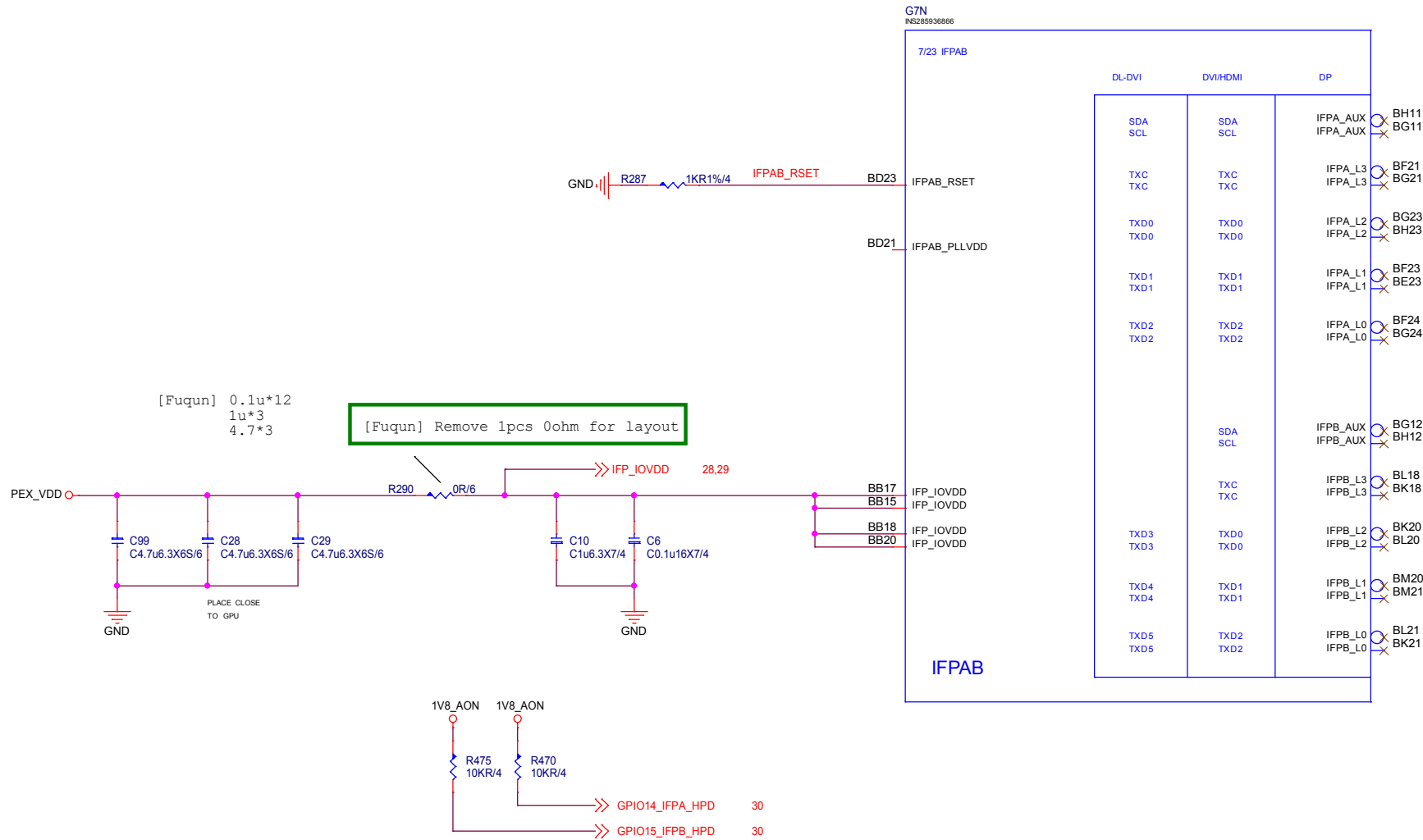
GPU DECOUPLING B

FBVDDQ
[Fuqun] 1u*22
10u*12
22u*9

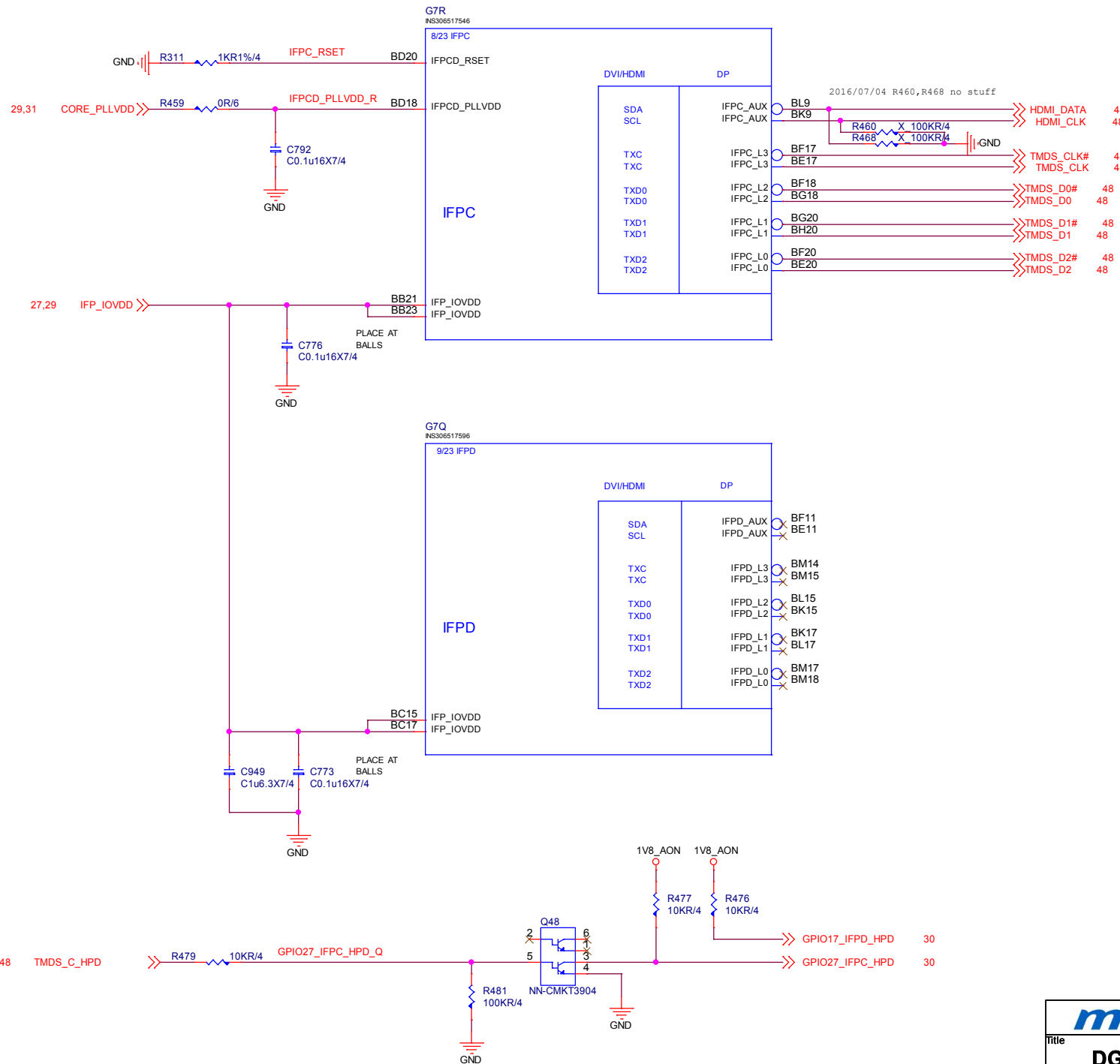


		MICRO-STAR INT'L CO.,LTD.	
Title			
DGPU GPU DECOUPLING B			
Size	Document	Number	Rev
		MS-16JC1	0B
Date:	Tuesday, October 18, 2016		Sheet 26 of 75

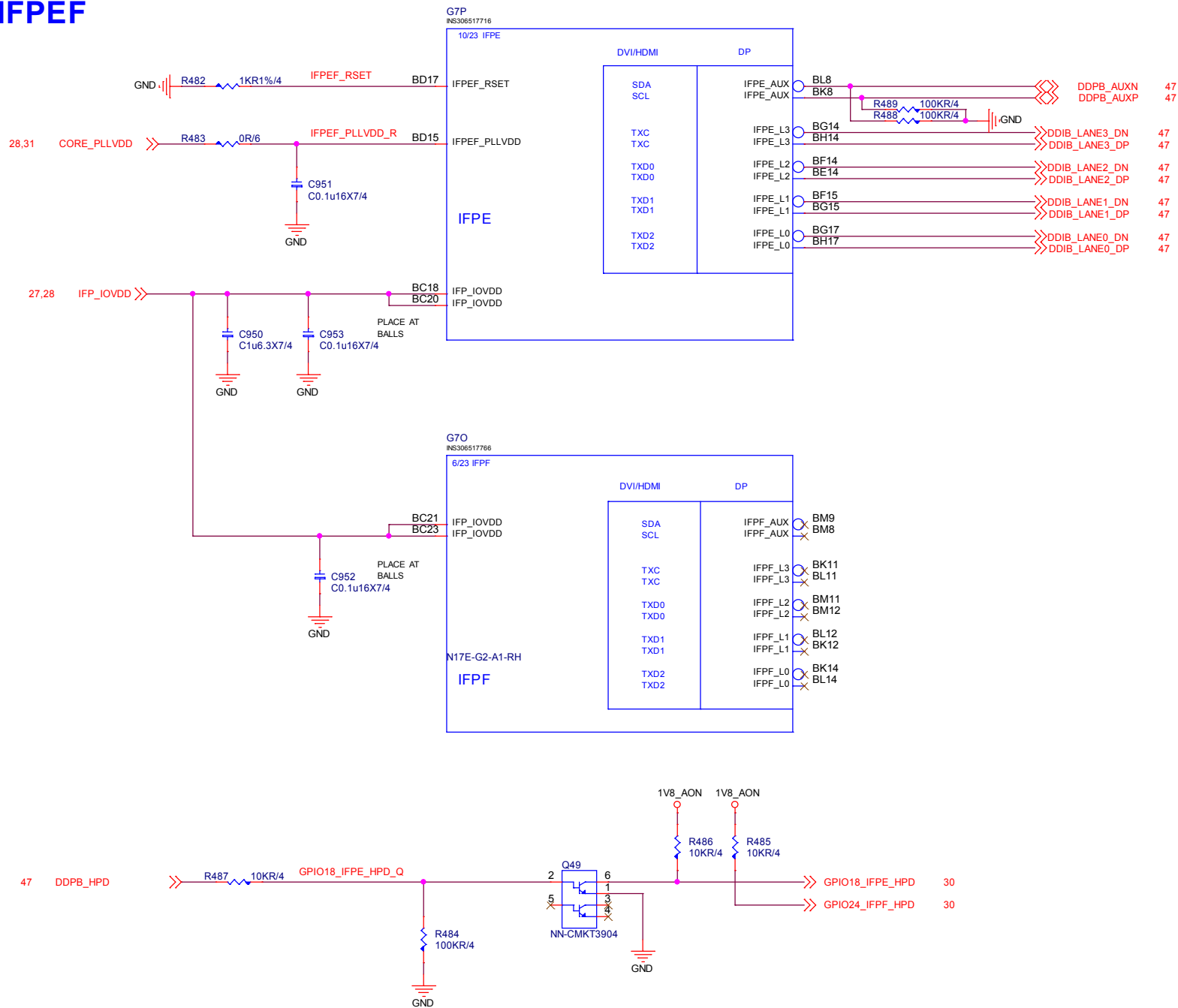
IFPCD



IFPCD



IFPEF

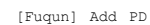
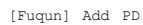


DP

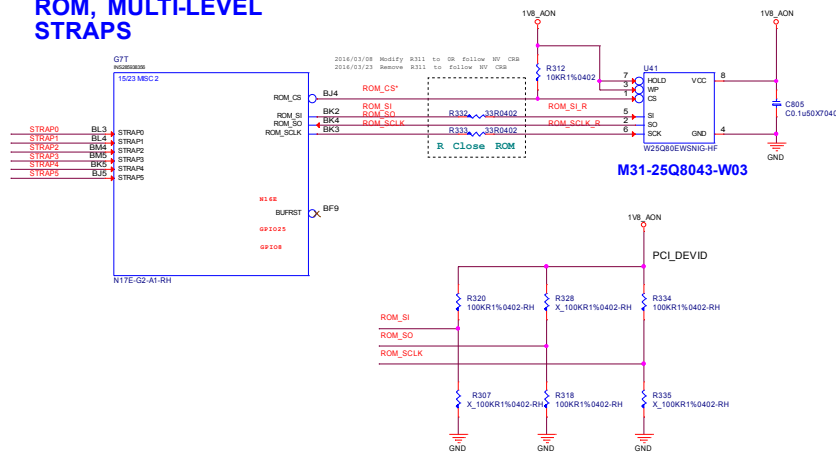
[Fuqun] Add R492



G7V
INS285937892



ROM, MULTI-LEVEL STRAPS



STRAP2 STRAP1 STRAP0 RAMCFG[4:0]

L	L	L	00000	0x0	Samsung: M12-8032535-S02 / K4G80325FB-HC25
L	L	H	00001	0x1	Micron: M12-2563215-M30 / MT51J256M32HF-80-A
L	H	L	00010	0x2	Hynix: 載
L	H	H	00011		
H	H	L	00110		H=High :Tied to 1.8V M=Middle:Tied to 0.9V L=Low :Tied to 0V
H	H	H	00111		

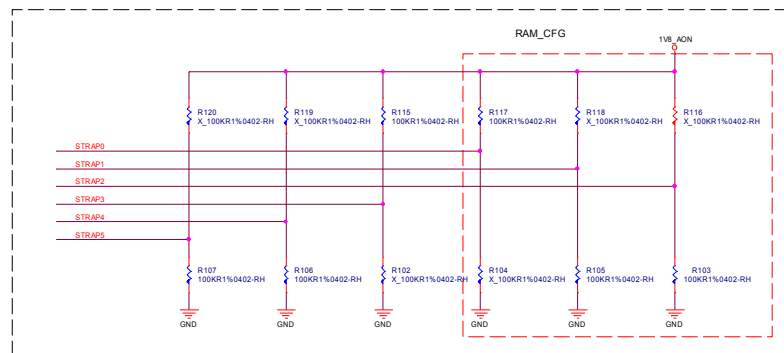
ROM_SO ROM_SI ROM_SCLK SOR_EXPOSED[3:0] 1:ENABLE 0:DISABLE

L	L	L	1111	DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110		
L	H	L	1101		
L	H	H	1100		
H	L	L	1011		
H	L	H	1010		
H	H	L	1001		
H	H	H	1000		
L	L	M	0111		
L	M	L	0110		
L	M	H	0101		
L	H	M	0100		
H	L	M	0011		
H	M	L	0010		
H	M	H	0001		
H	H	M	0000		V

STRAP5 STRAP4 STRAP3 SMB_ALT_ADDR DEVID_SEL PCIE_CFG VGA_DEVICE

M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

1.SMB_ALT_ADDR ENABLE
0.SMB_ALT_ADDR DISABLE
1.DEVID_SEL REBRAND
0.DEVID_SEL ORIGINAL
1.PCIE_CFG LOW POWER
0.PCIE_CFG HIGH POWER
1.VGA_DEVICE ENABLE
0.VGA_DEVICE DISABLE



DEFAULT SETTING BOT 備註頂欄

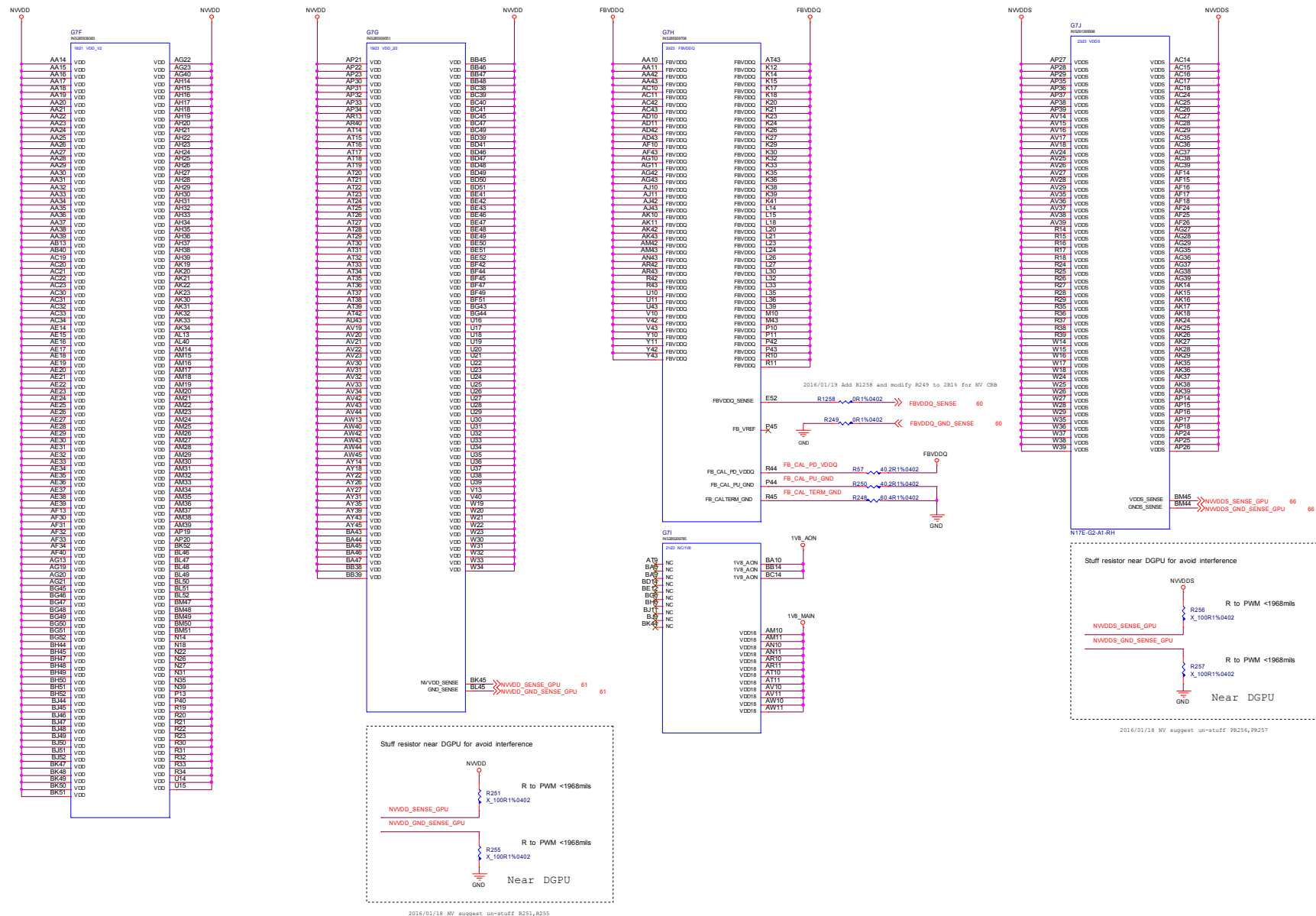
V_BOOT1	Samsung
M12-8032535-S02	256Mx32bit
X_K4G80325FB-HC25	
V_BOOT2	Hynix
M12-56C2H05-H23	128Mx16bit
X_H5GQ2H24BFR-T2C	

Item		N17E-G2	N17E-G1
Device ID		1BA1	1C20
Package		GB4-256	GB4-256
Internal P/N			
ROM_SO	0x0: HHM (all disabled)	low	low
ROM_SI	0X12:LHH	High	High
ROM_SCLK	0X12: LHH 16B/16/C	High	High
Strap2	0x0: L L L		
Strap1	0x1: L L H		
Strap0	0x2: LHL		
Strap5	0000 =optimus, LLL	low	Low
Strap4	0001= discrete, LLH	low	Low
Strap3	0101=discrete with Gsync, HLH	high	high
NVDD Boot Voltage	0.8V	0.8v	0.8v

Table 1. N17E-G1/-G2 GDDR5 Recommended Memories

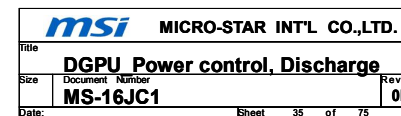
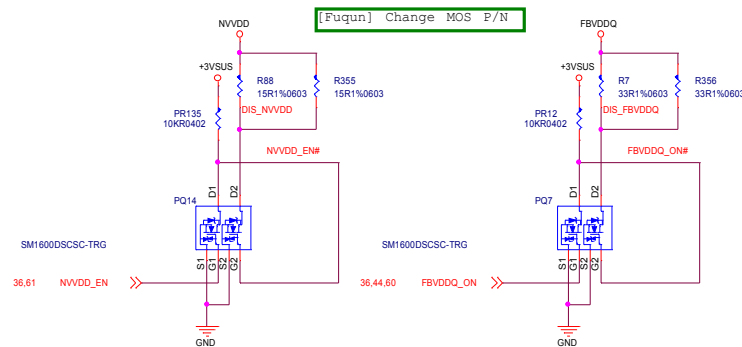
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V ²	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V ²	Micron	MT51J256M32HF-80-A	A-die	0x1	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V ²	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production candidate

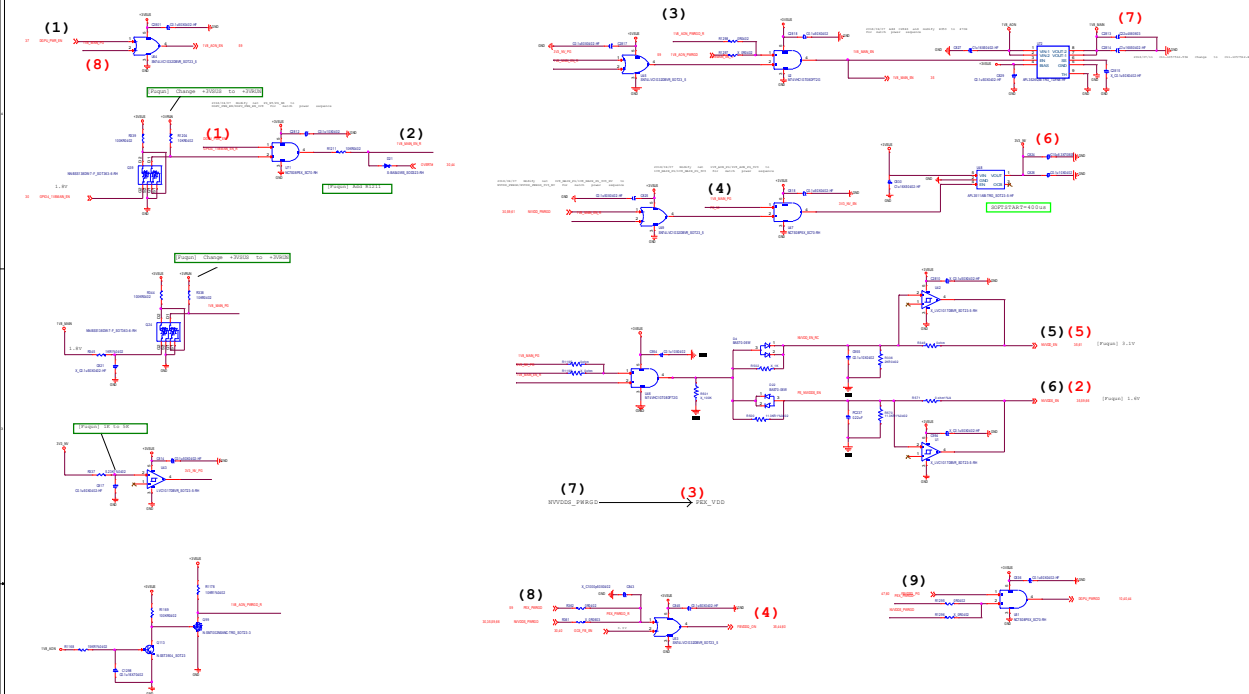
GPU NVVDD, FBVDDQ



[illegible]

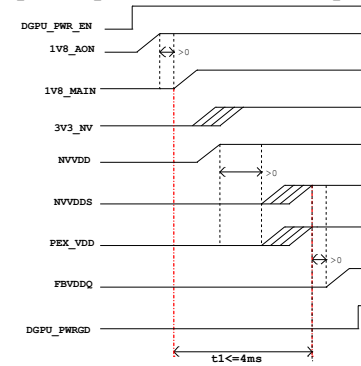
DGPU_Power Control





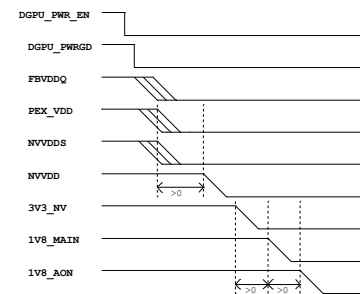
POWER UP Sequence

1V8_AON -> 1V8_MAIN->NV3V3 -> NVVDD -> NVVDDSD / PEX_VDD -> FBVDDQ

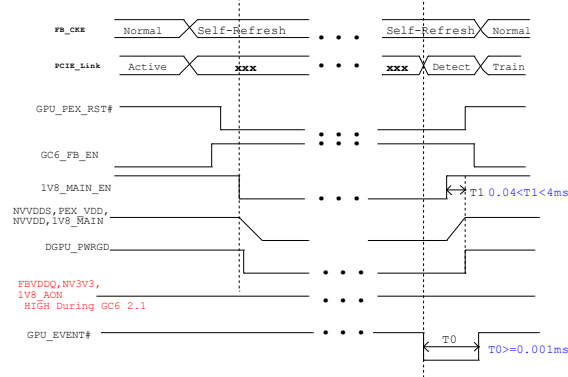


POWER Down Sequence

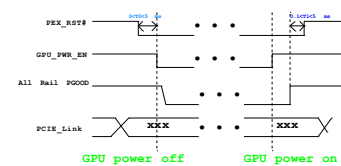
NVVDDSD/PEX_VDD/FBVDDQ ->NVVDD/NV3V3->1V8_MAIN-> 1V8_AON

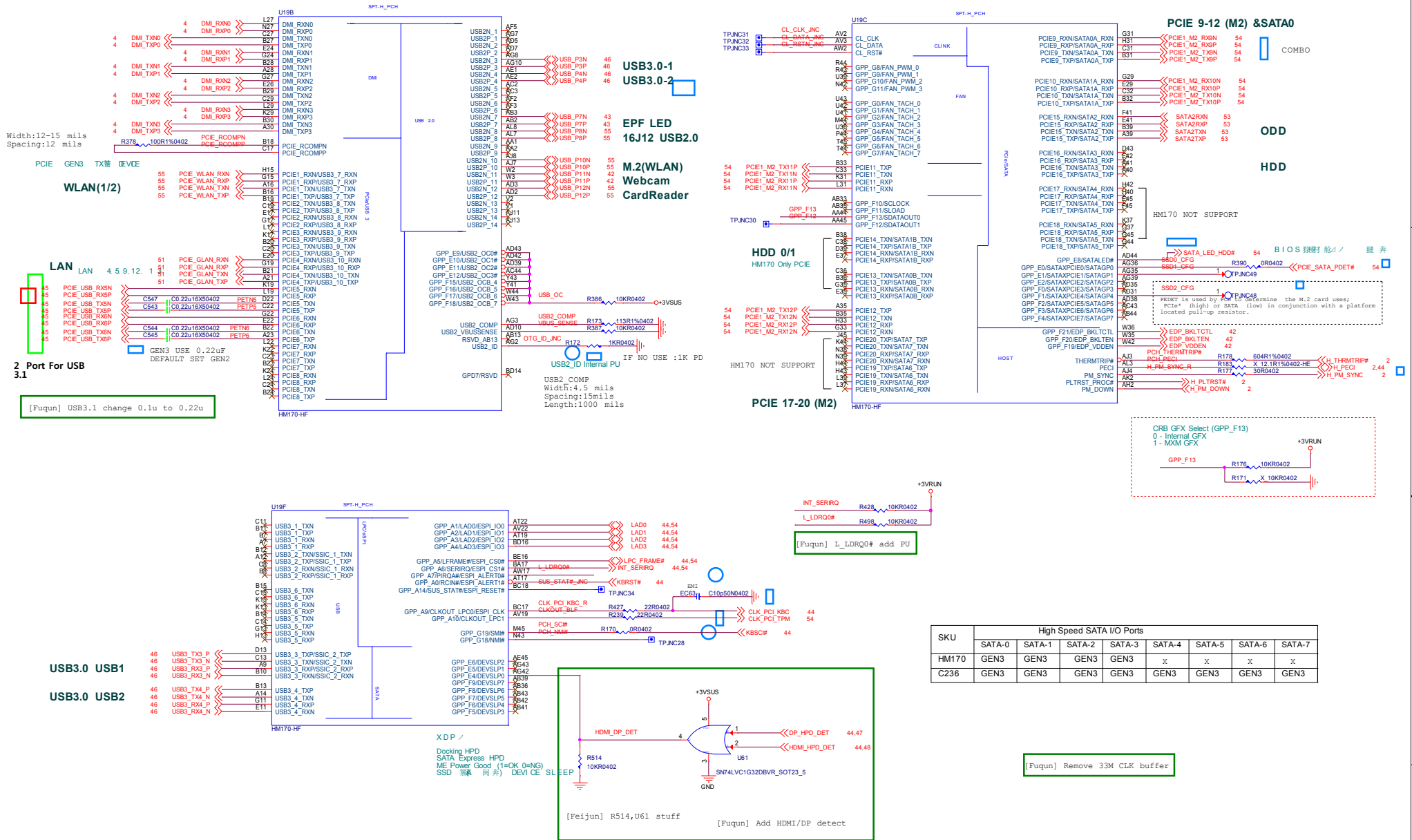



GC6 2.1 Entry/Exit Timing

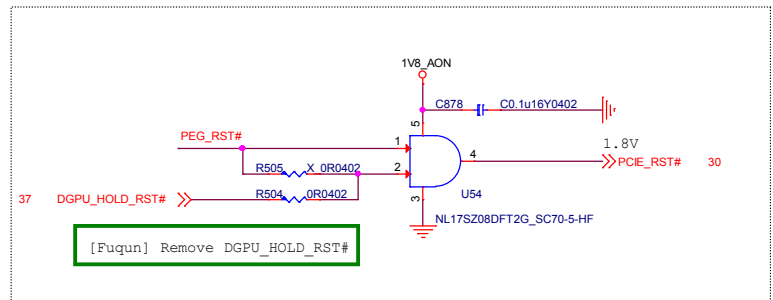
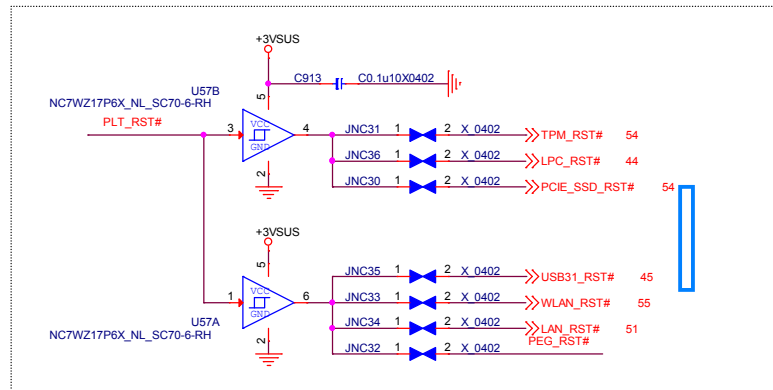
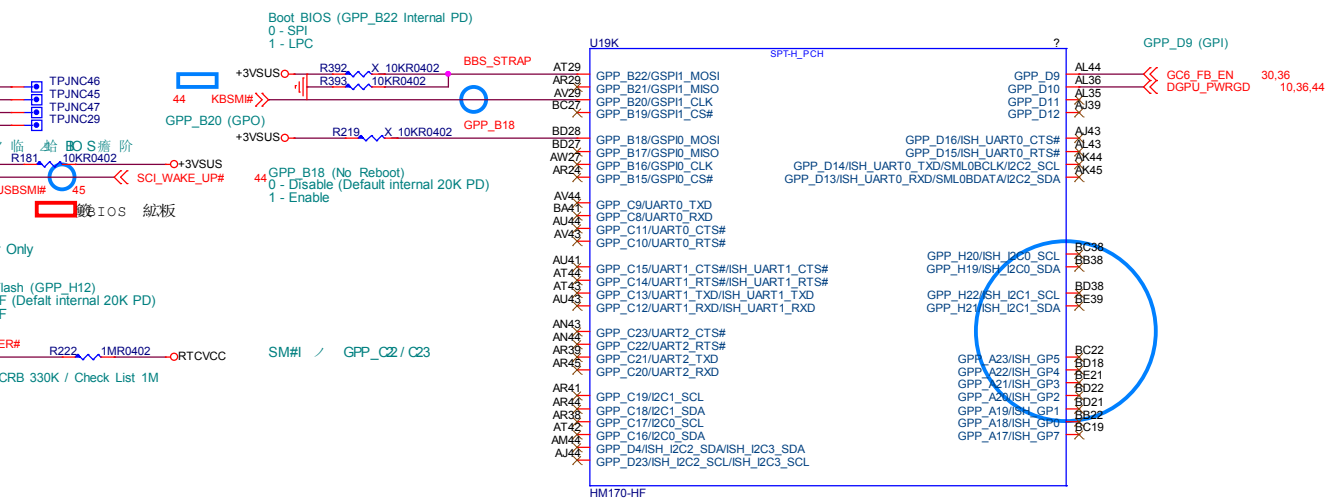
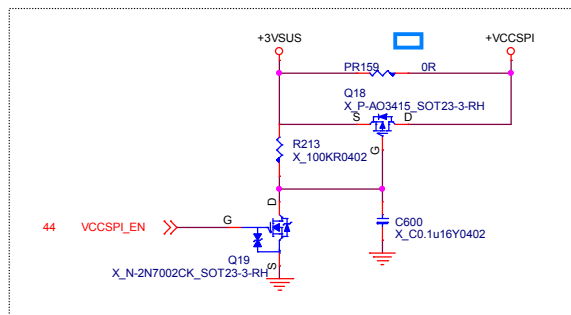
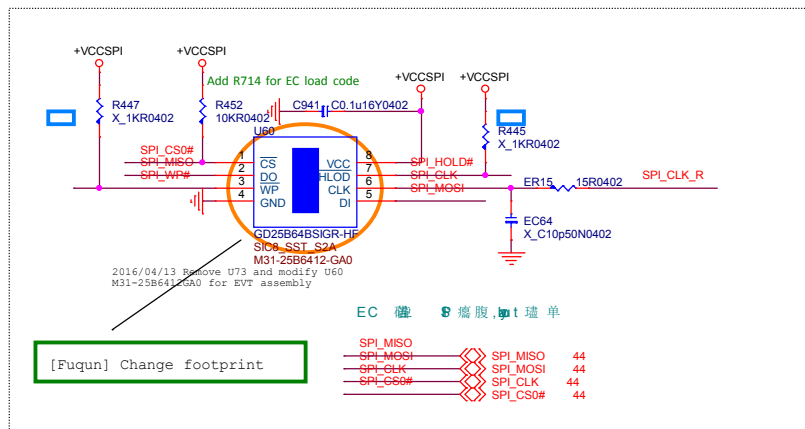
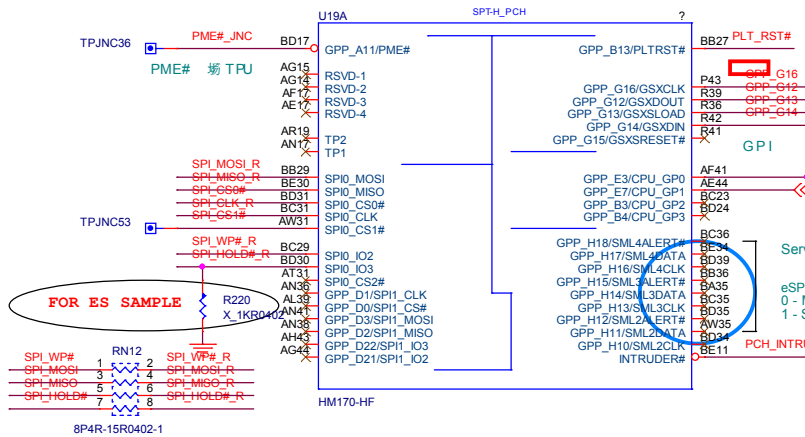


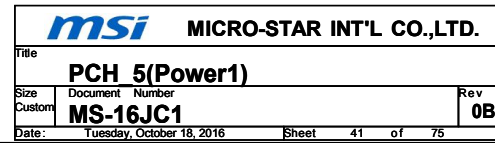
Optimus Entry/Exit Timing Diagram





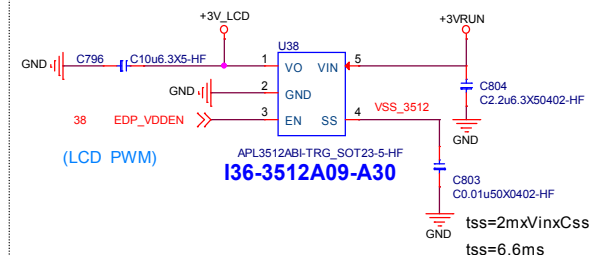
		MICRO-STAR INT'L CO.,LTD.	
Title			
PCH 3(HDA/RTC/SMBUS)			
Size	Document	Number	Rev
Custom	MS-16JC1		0B
Date:	Tuesday, October 18, 2016	Sheet	39 of 75



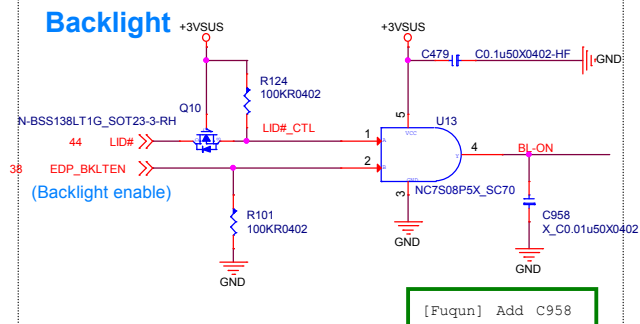


eDP

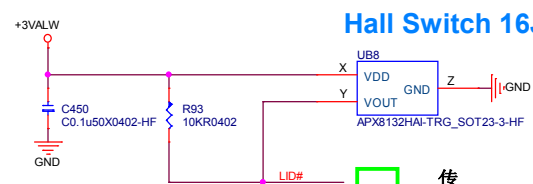
Pannel Device Logic Power



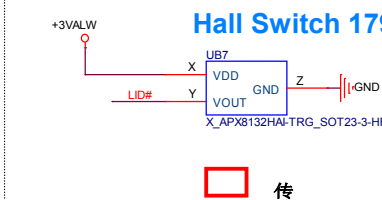
Backlight



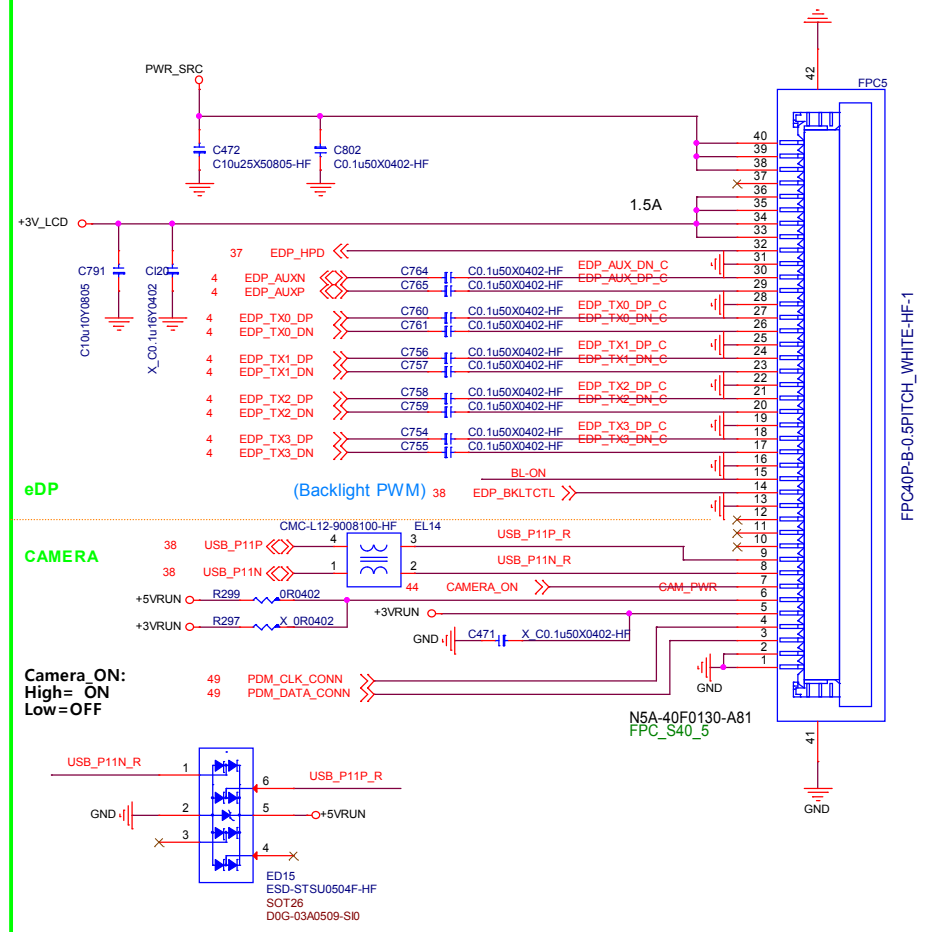
Hall Switch 16JC



Hall Switch 179C



eDP CONN CAMERA



LCD Module Pin Define

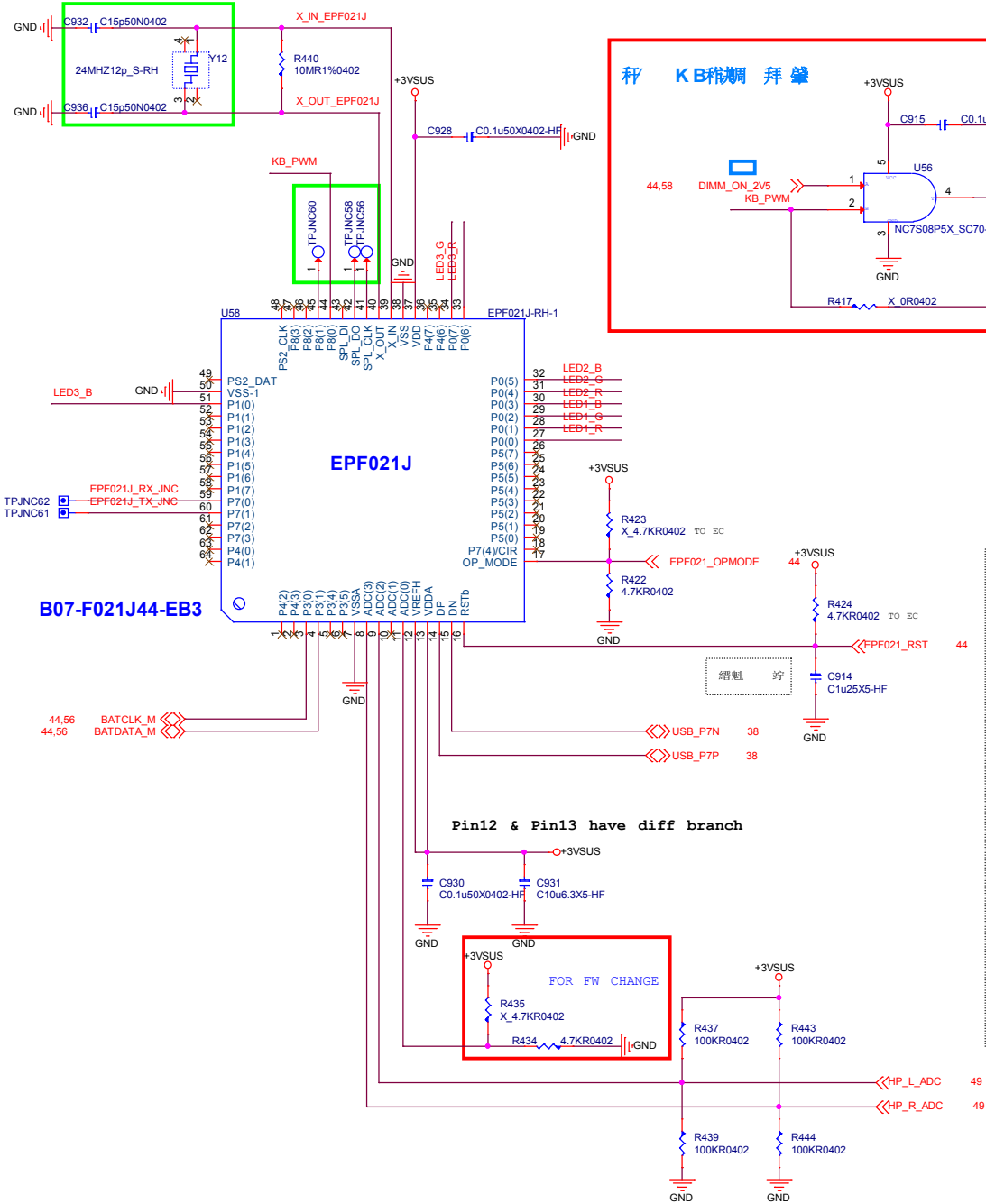
Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDI	HPDI signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

msi MICRO-STAR INT'L CO.,LTD.

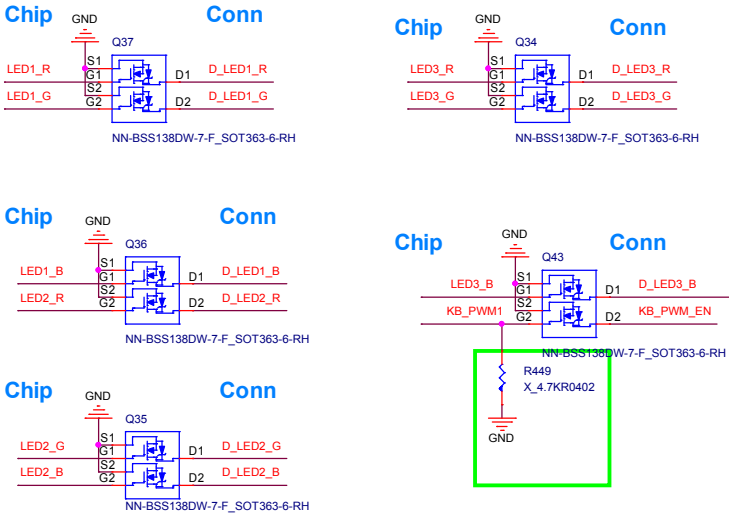
Title		
eDP /Camera		
Size	Document Number	Rev
	MS-16JC1	0B
Date:	Tuesday, October 18, 2016	Sheet 42 of 75

LED 8051 Controller

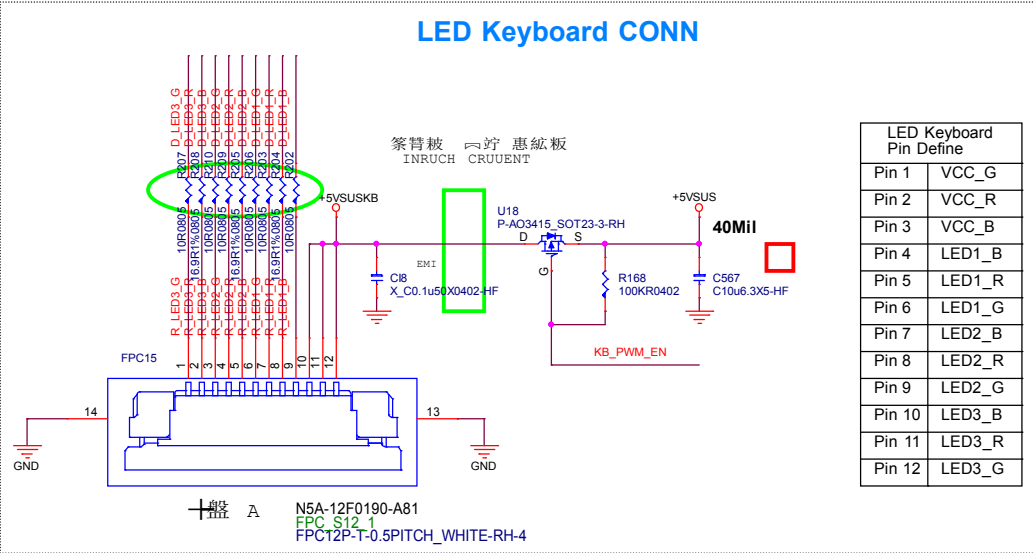
C749 and C750 change to 15pF for SA



EPF021J Sink current not enough, only using BSS138 (0.22A)



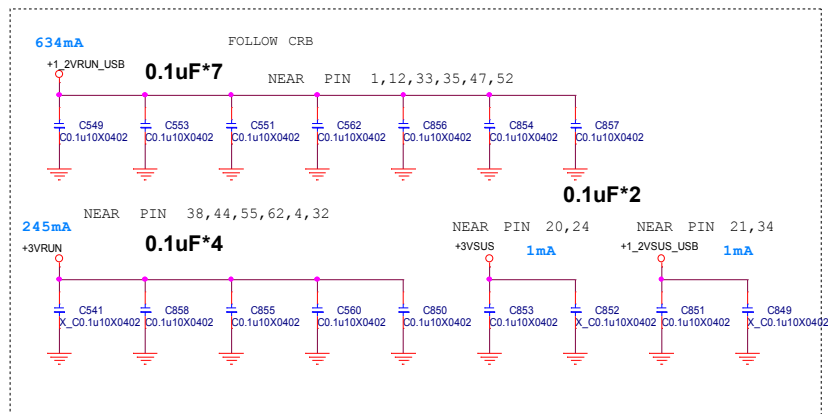
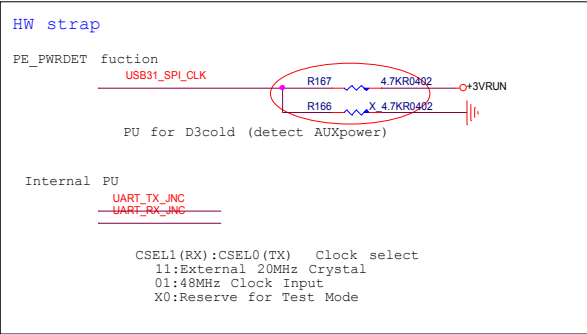
LED Keyboard CONN



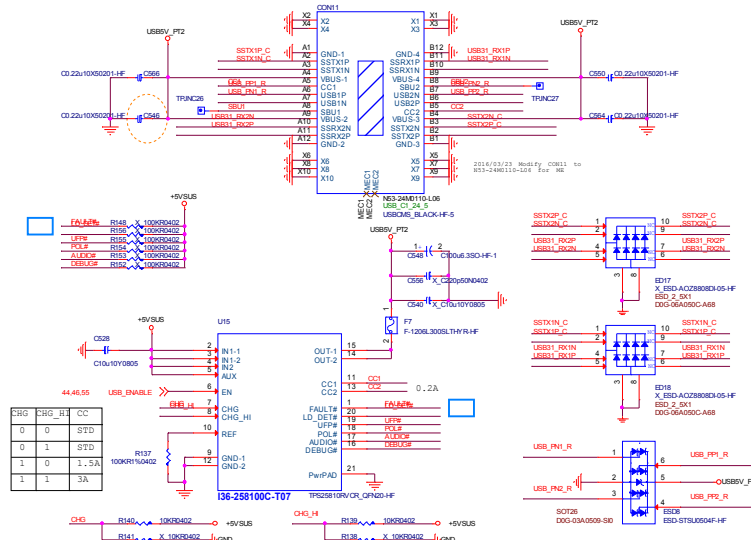
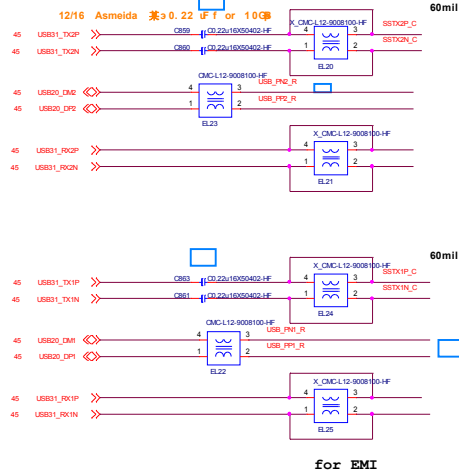
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

Tuesday, October 18, 2016 Sheet 44 of 75

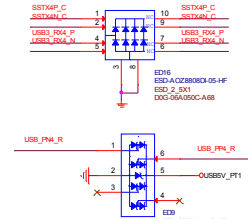
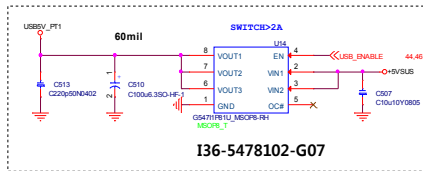
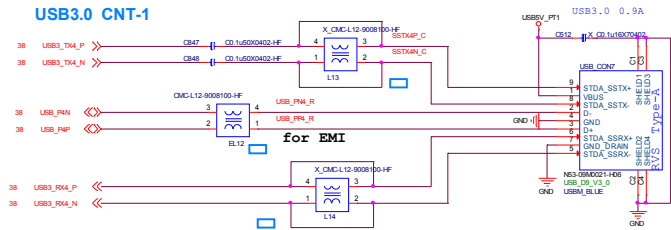
PCIE to USB 3.1



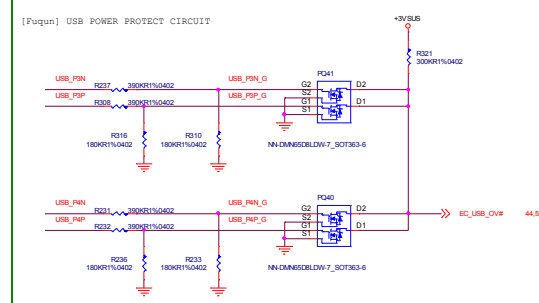
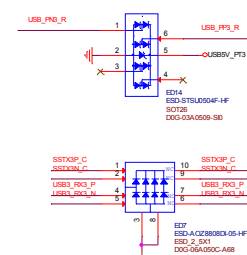
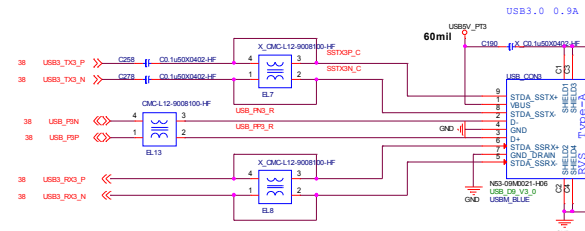
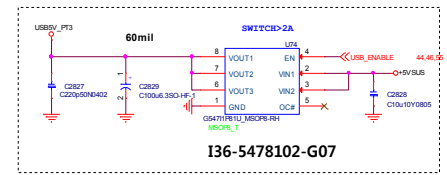
USB3.1 TYPE C



USB3.0 CNT-1



USB3.0 CNT-3



[Fuqun] Add MOS 1.0

2016/07/04 R068,R588 atufef

3V3_VV

R1 2KRD402

R5 2KRD402

R3 XDRD402

R13 DRD402

C0.01/10RD402

C1

GND

G2

G1

S1

Q1

O2

D1

HDMI_CLK_B

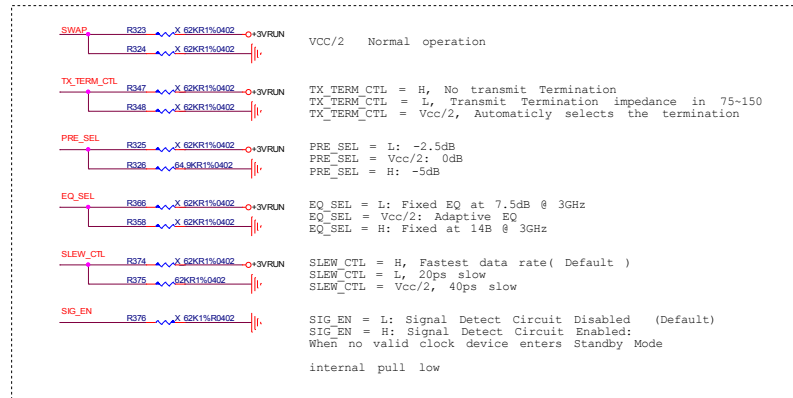
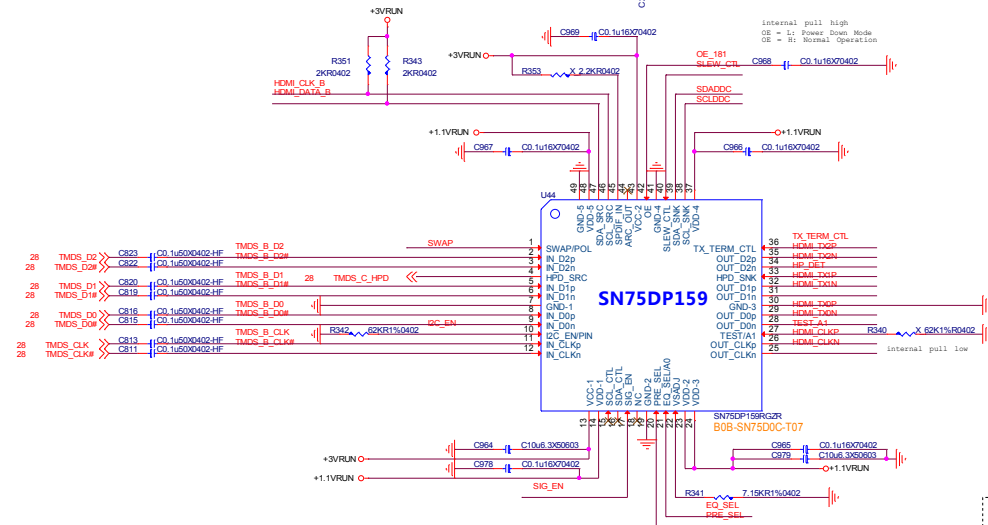
HDMI_DATA_B

SM1600DS-CSC-TRG

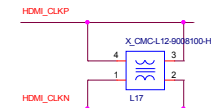
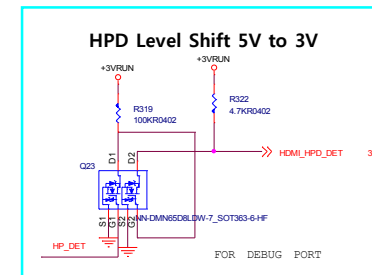
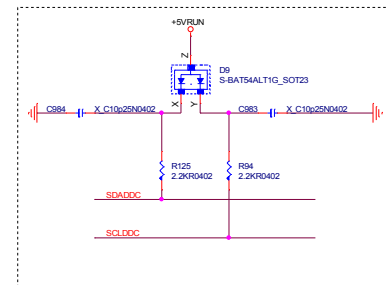
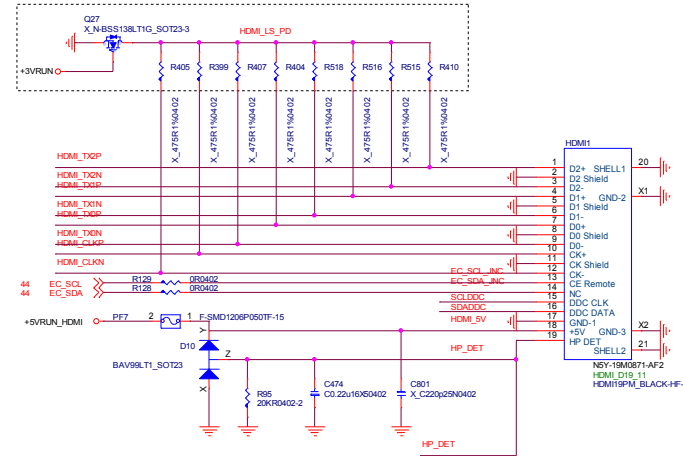
47

28 HDMI_CLK

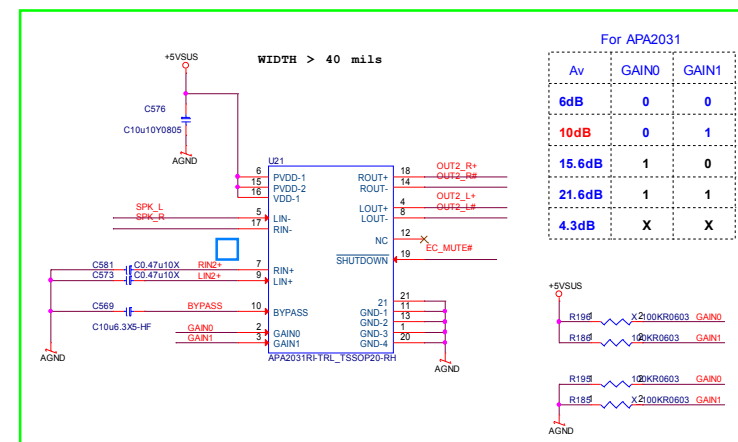
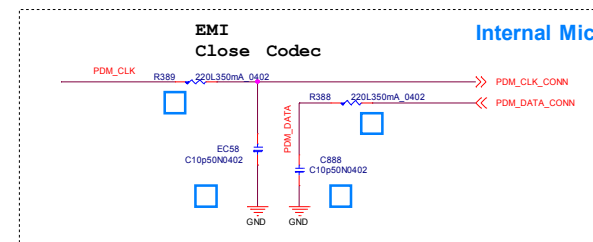
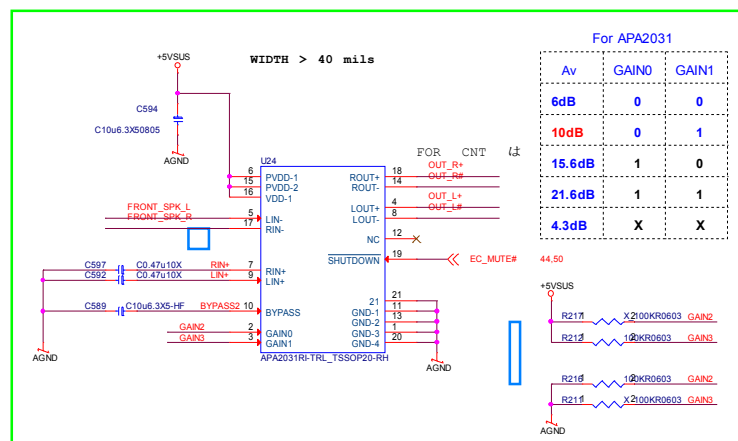
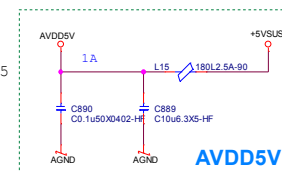
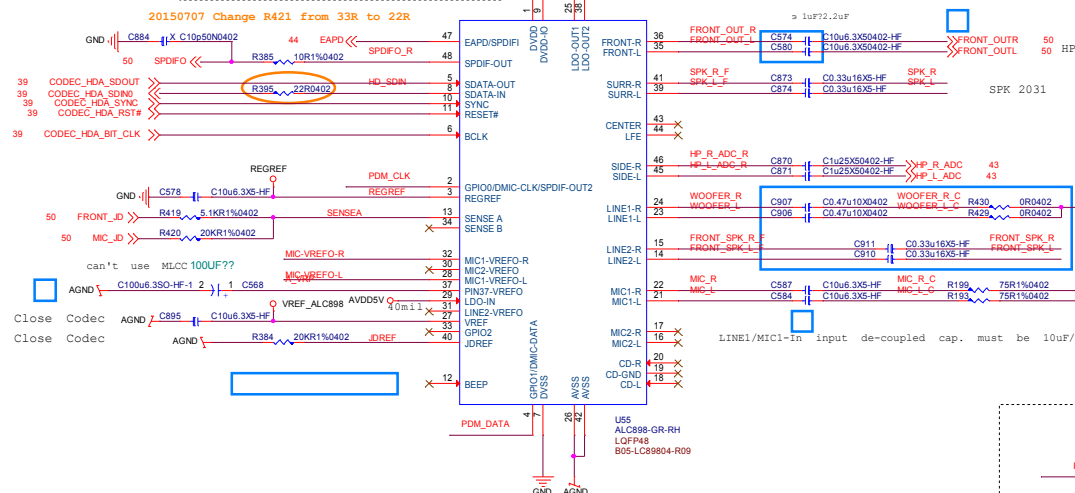
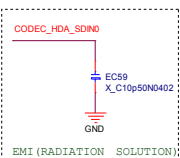
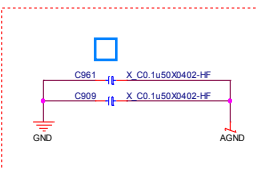
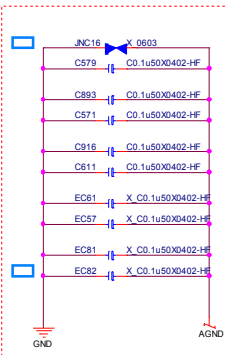
28 HDMI_DATA



P159	NC
S181	Stuff



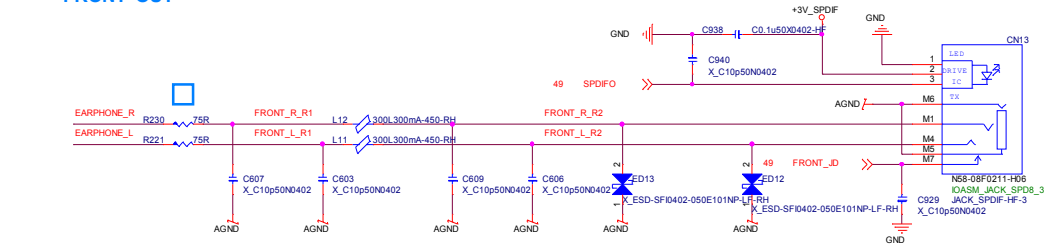
閣MOA 篠 十 COOPER



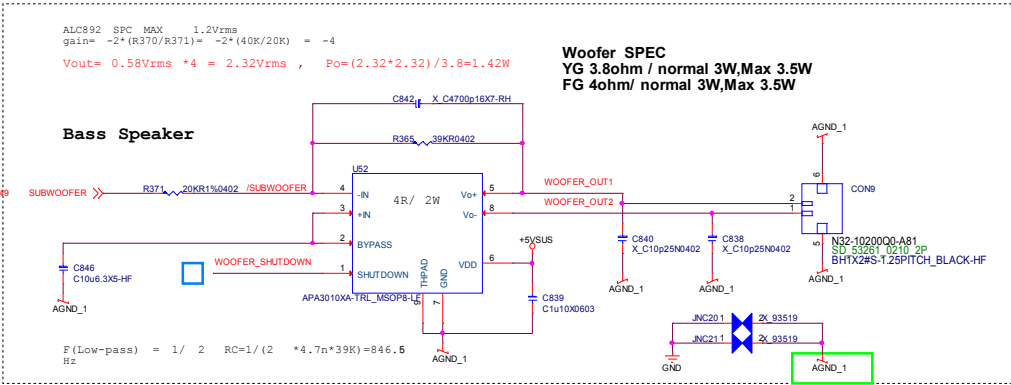
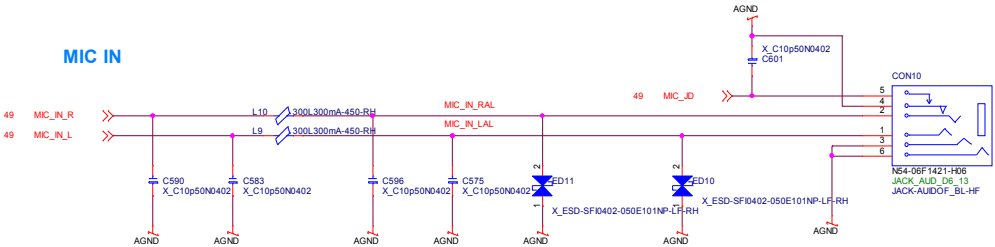
	CODEC	斥
L	-	-
L	+	+
R	+	+
R	-	-
L2	+	+
L2	-	-
R2	-	-
R2	+	+

Audio CONN /Woffer

FRONT OUT

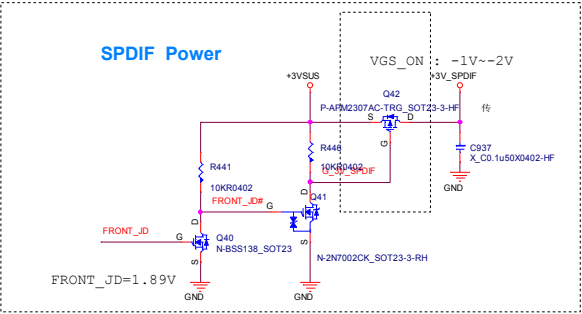


MIC IN

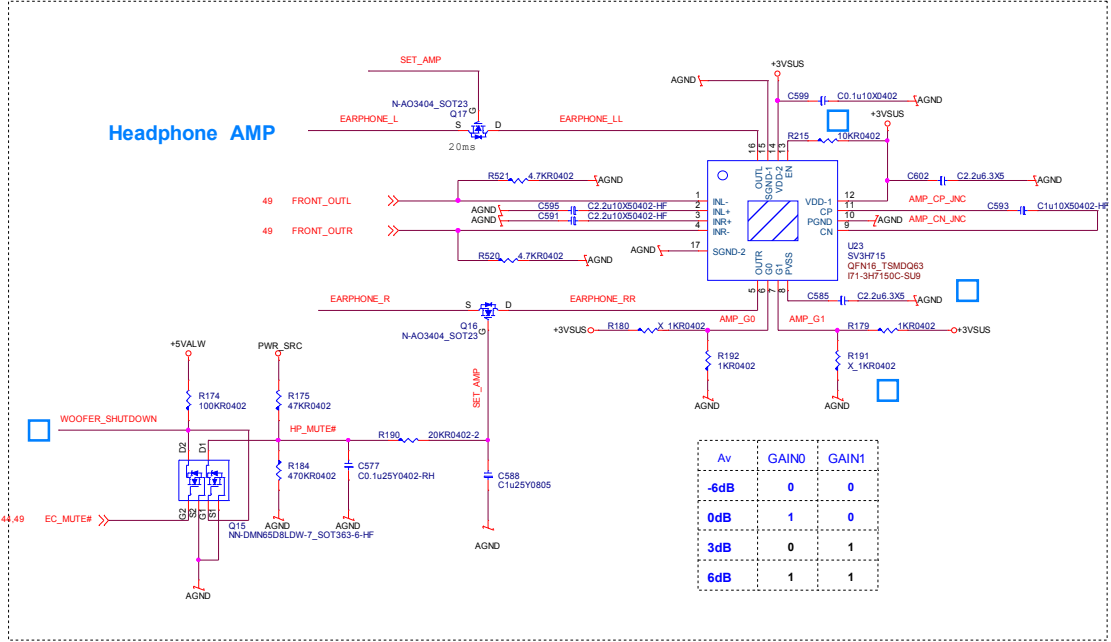


WOOFER AMP 驛ミちA GN D_ 1

SPDIF Power

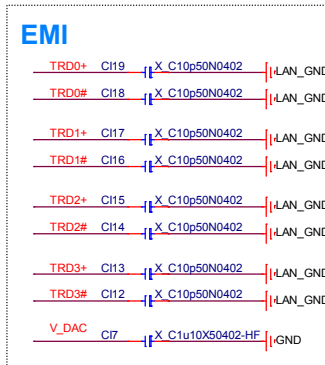
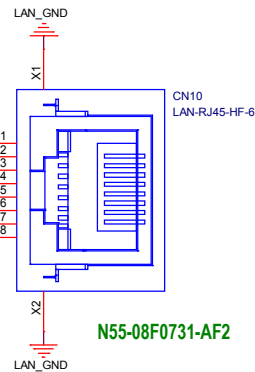
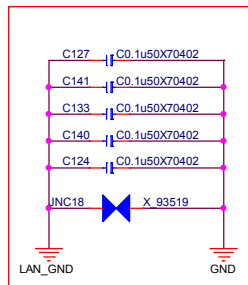
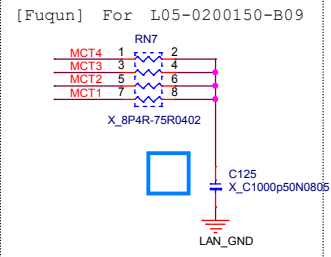
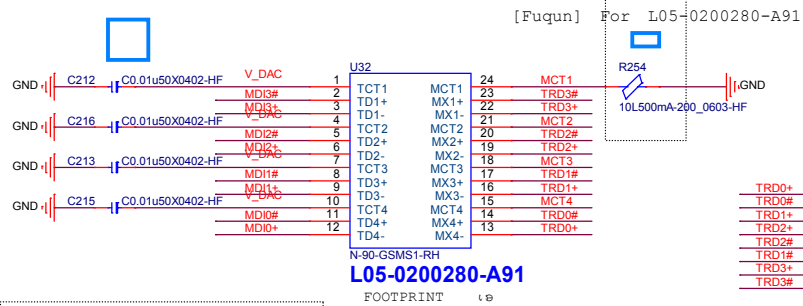
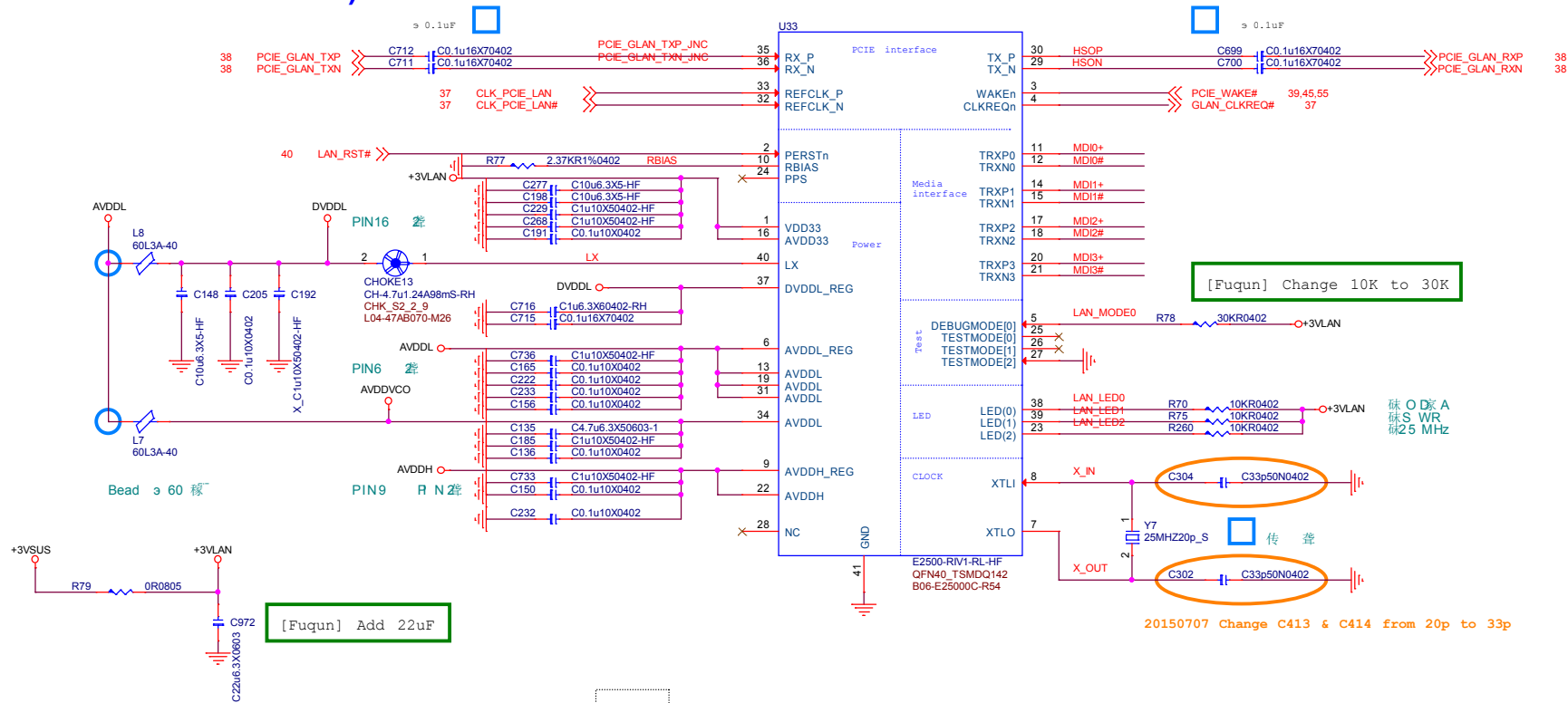


Headphone AMP

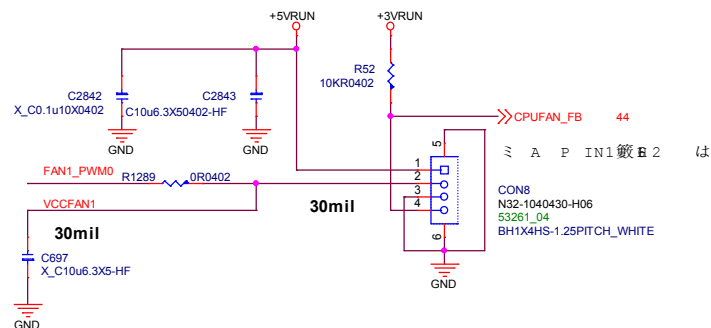
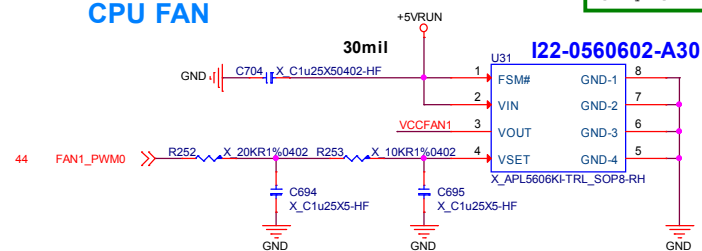


Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

GIGA LAN(BigFoot BFN2400B)

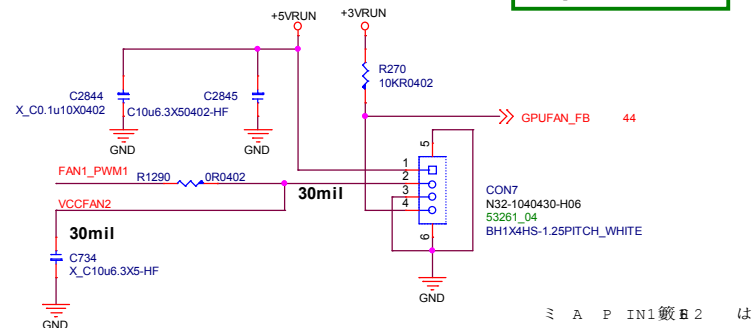
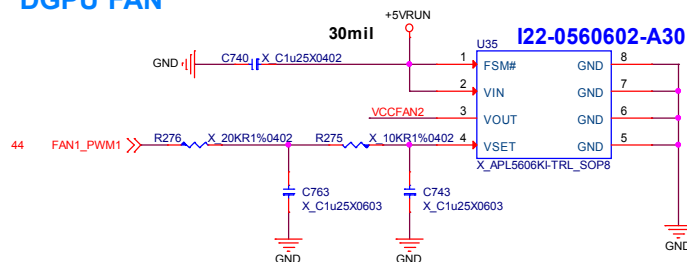


CPU FAN



	Stuff parts	Un-stuff parts
PWM	R1289	R252,R253,C694,C695,c697
D Δ AR	R252,R253,C694,C695,c697	R1289

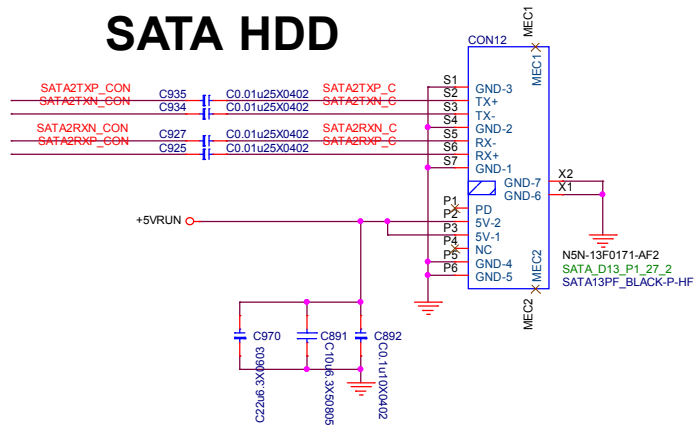
DGPU FAN



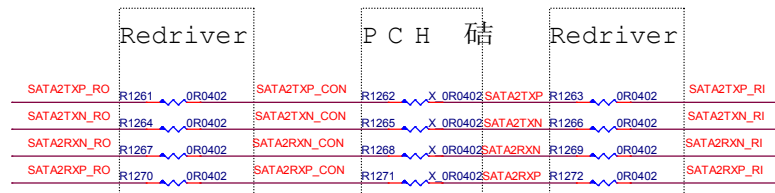
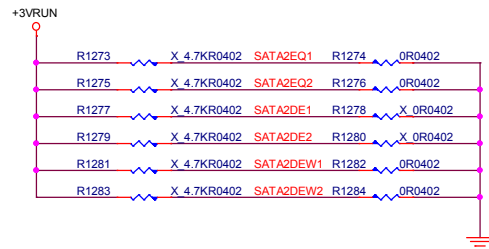
	Stuff parts	Un-stuff parts
PWM	R1290	R276, R275, C763, C743, C734
D Δ AR	R276, R275, C763, C743, C734	R1290



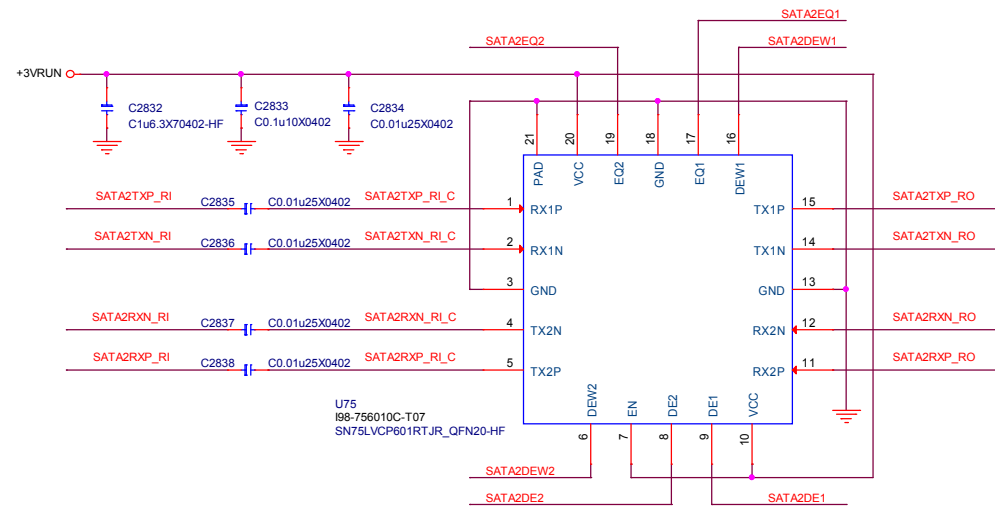
SATA HDD



[Fuqun] Add 22uF



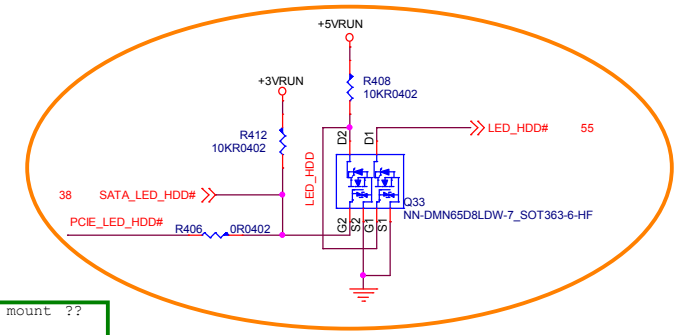
Verge HDD reDRIVER



TX and RX EQ and DE Pulse-Duration Settings

DE1 OR DE2	CH1 OR CH2 DE-EMPHASIS dB (at 6 Gbps)	EQ1 OR EQ2	CH1 OR CH2 Equalization dB (at 6 Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14
DEW1 OR DEW2	DEVICE FUNCTION → DE WIDTH FOR CH1/CH2		
0	De-emphasis pulse duration, short		
1 (default)	De-emphasis pulse duration, long		

[Fuqun] Change ??



STAND OFF

H8
Spacer
Support

E2B-16J1010-RH

H=4.15

38,44 LAD0 26 LAD0 GPIO 6 +3VRUN
 38,44 LAD1 23 LAD1 19
 38,44 LAD2 17 LAD2 24 VDD-1
 38,44 LAD3 15 LAD3 10 VDD-3
 38,44 LFRAME# 22 LFRAME# 5 VDD-4
 40 TPM_RST# 18 LRESET# 18
 38,44 INT_SERIRQ 15 NC-1 25
 38 CLK_PCL_TPM 27 NC-2 11
 21 SERIRQ 4 GND-2
 9 LCLK 18 GND-3
 8 NC-3 14
 7 NC-4 13
 2 PP NC-8
 1 NC-5 12
 2 NC-6 3
 1 NC-9
 1 NC-10

U25
 X_SL69685TT2.0-RH-1
 TSSOP28
 B0C-0966512-114

R234
 X_10KR0402
 R235
 X_10KR0402
 R238
 X_4.7KR0402
 R239
 X_4.7KR0402

+3VRUN
 +3VRUN
 +3VRUN

C608 X C0.1u16Y0402
 C615 X C0.1u16Y0402
 C610 X C0.1u16Y0402
 C616 X C0.1u16Y0402

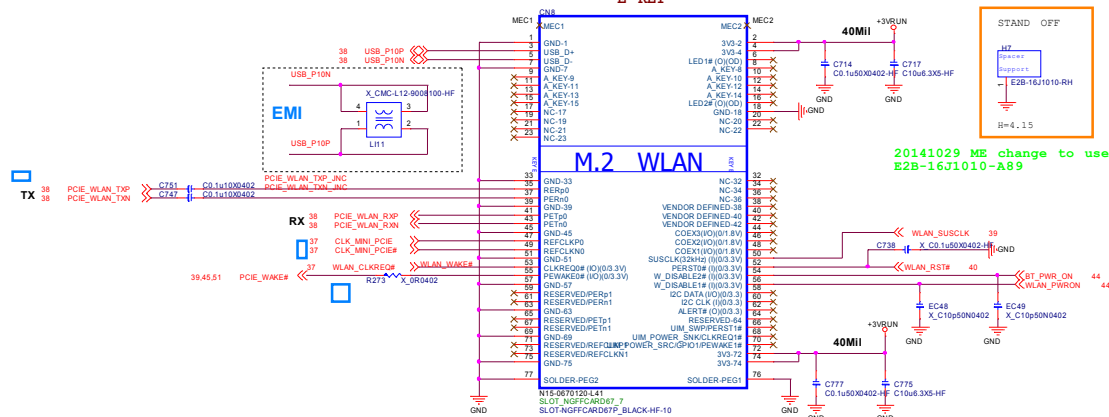
2016/07/08 Modify U25,R235,C608,C610,C615,C616 to stuff for DVT request

2016/07/08 Modify U25,R235,C608,C610,C615,C616 to stuff for DVT request

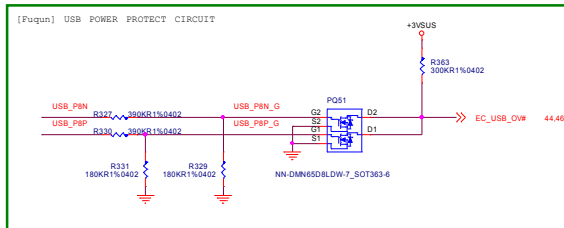
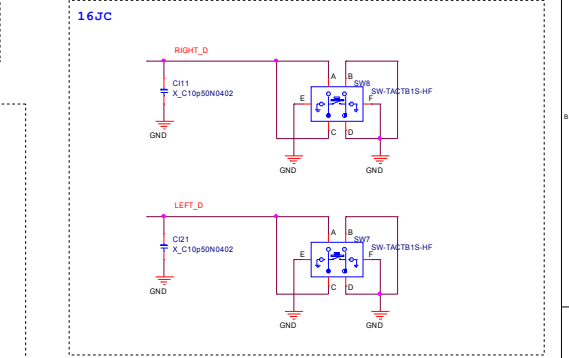
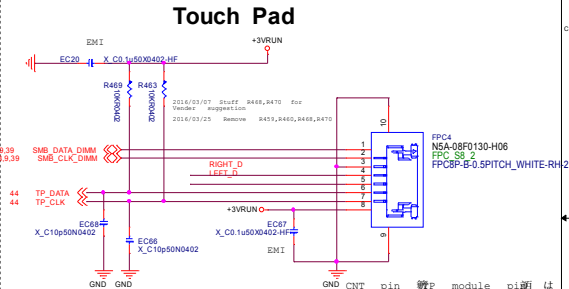
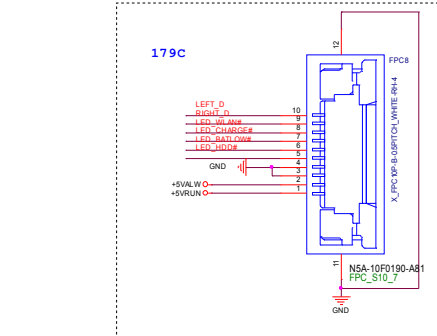
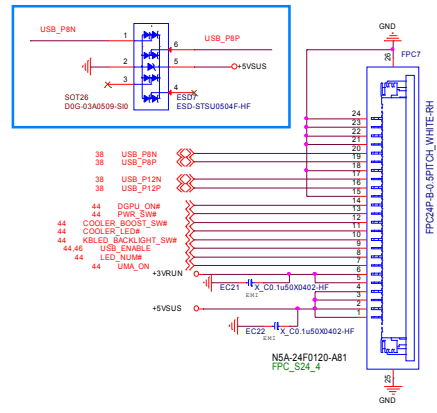
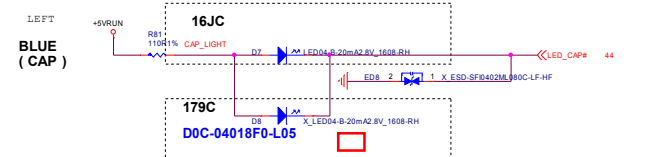
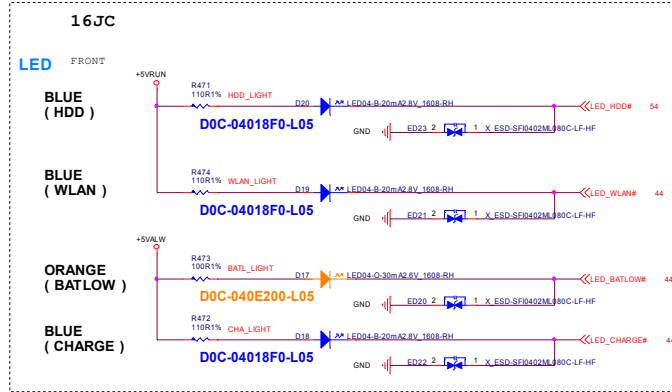
WLAN

WLAN/LED

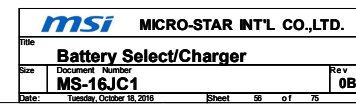
E KEY



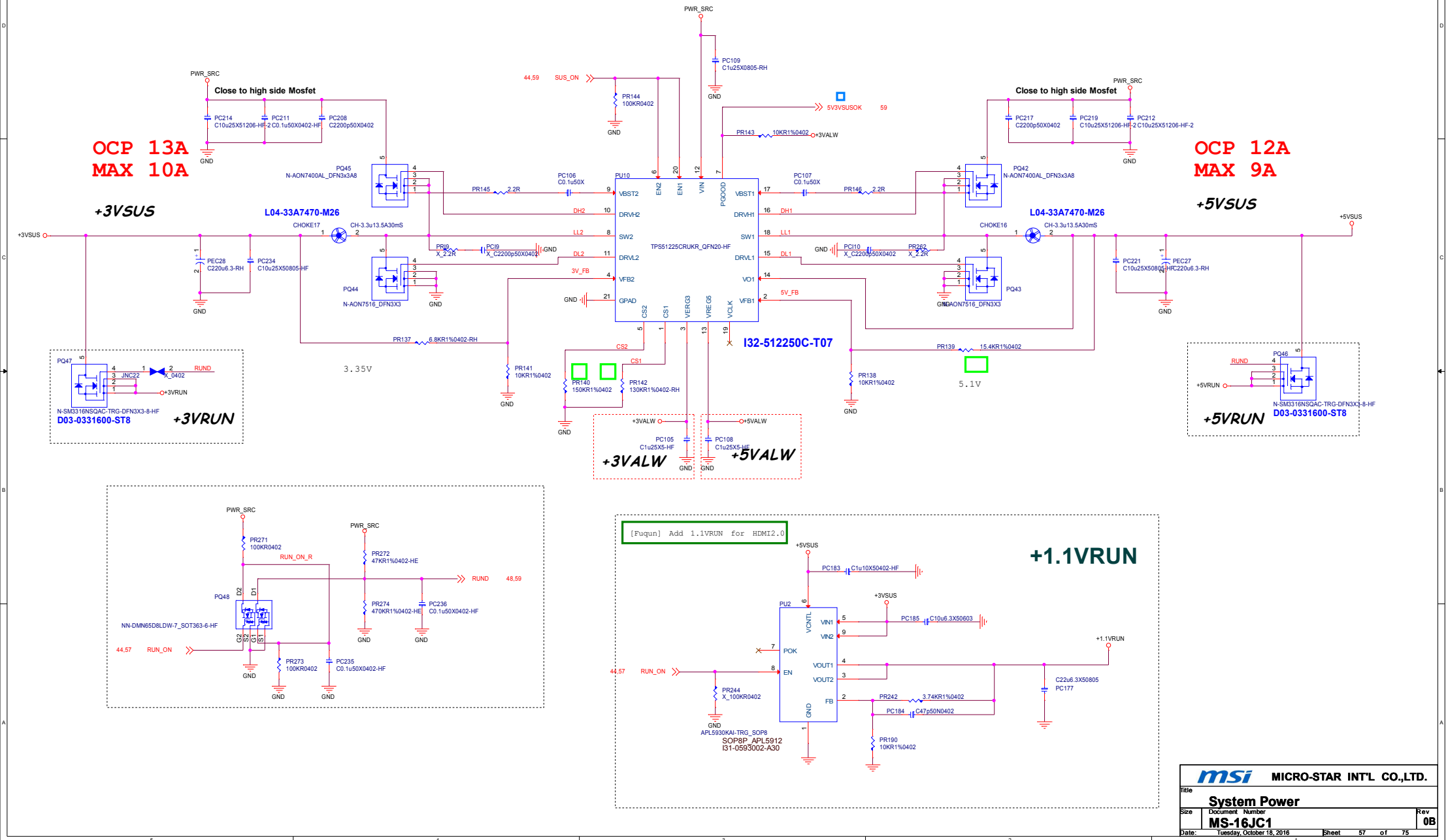
Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1# Module Key
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	BT EN (TW_DISABLE2#)
Pin 53	CLKREQ0#	Pin 54	BT EN (TW_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN (TW_DISABLE2#)
Pin 57	GND	Pin 58	WLAN_EN (TW_DISABLE2#)
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	N/C	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	N/C	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	N/C		

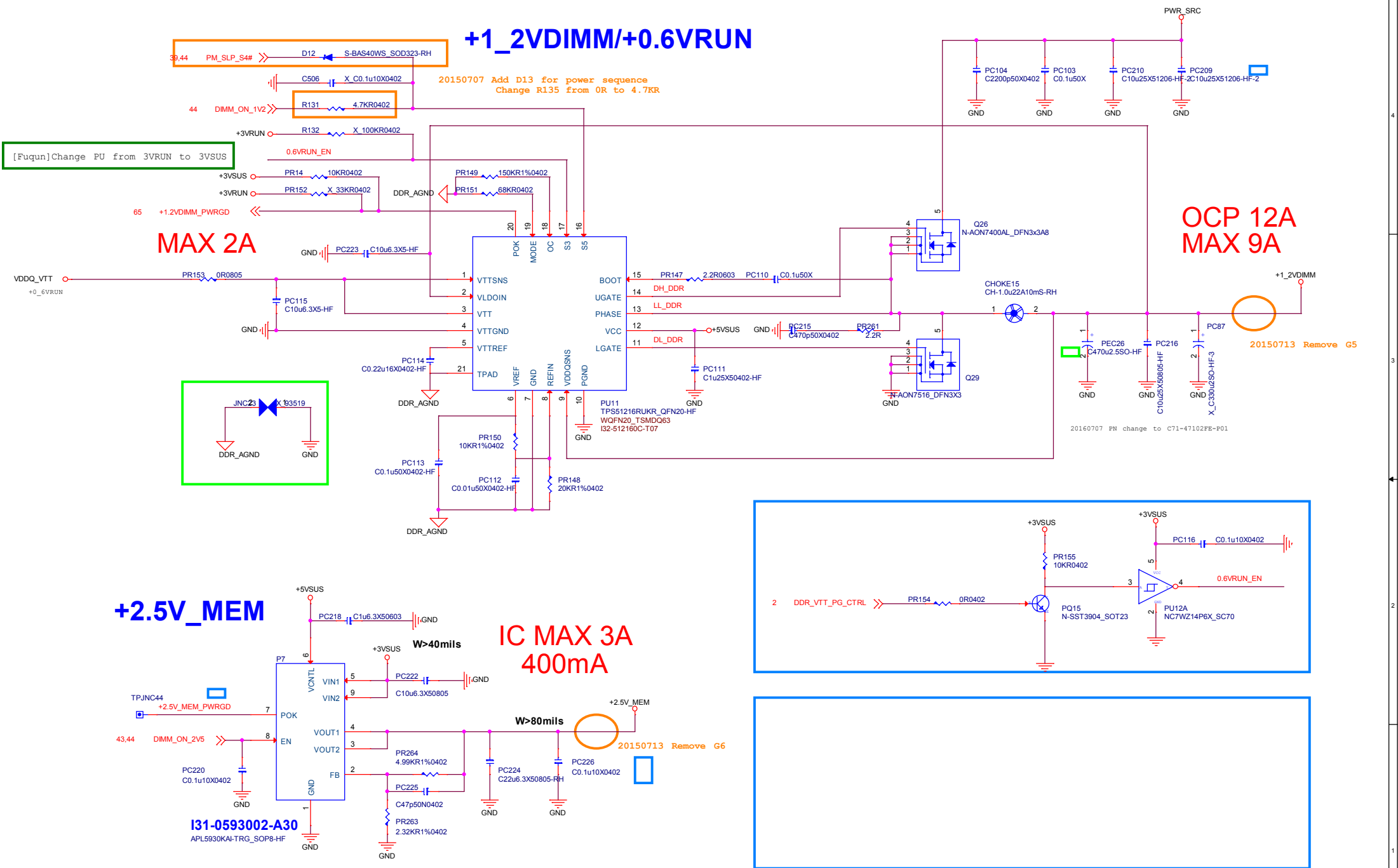


Battery Select/Charger

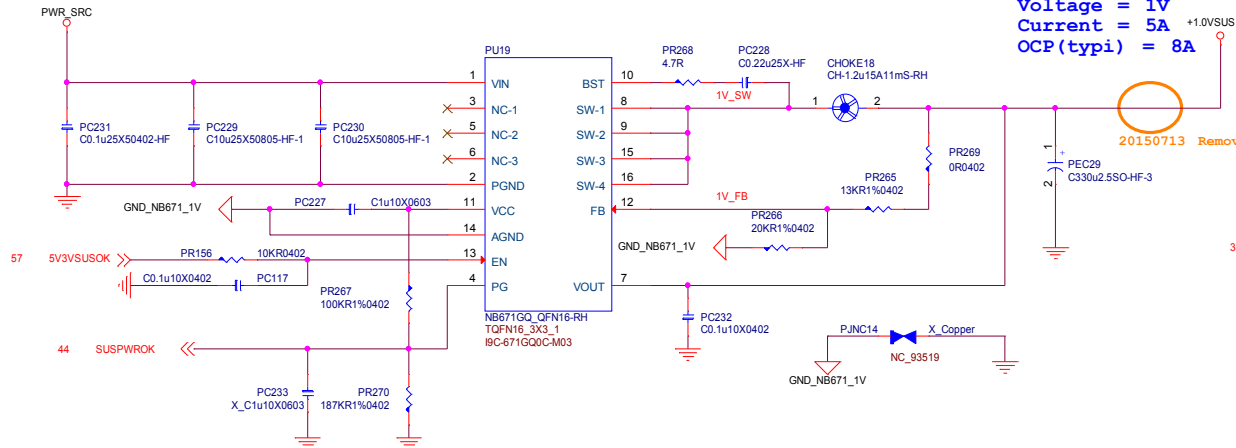


System Power



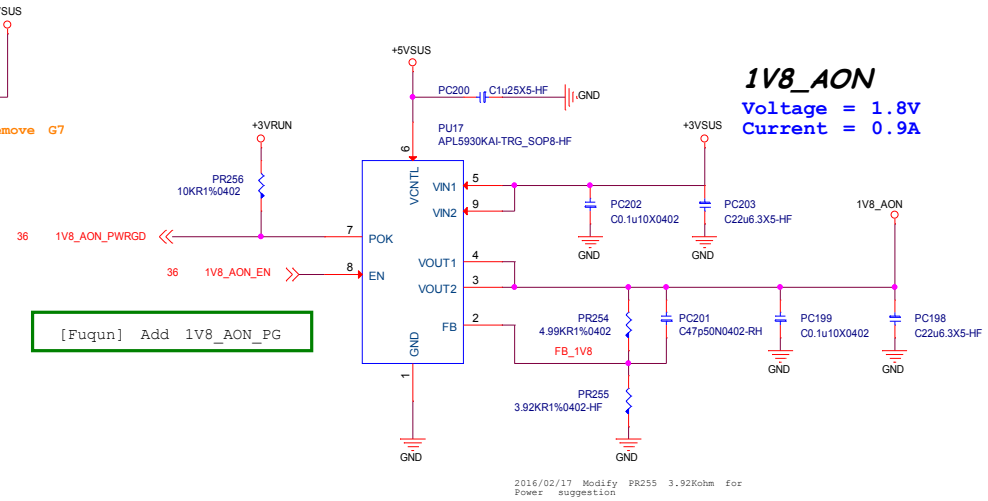


+1VSUS



+1.0VSUS

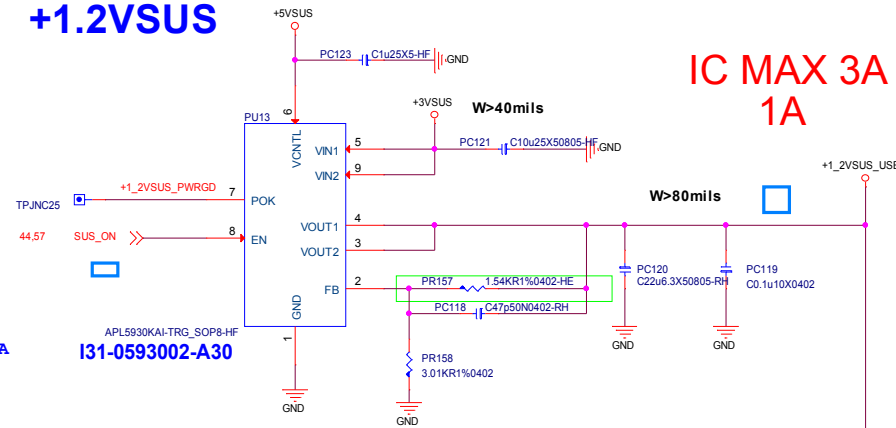
Voltage = 1V
Current = 5A
OCP(typi) = 8A



1V8_AON

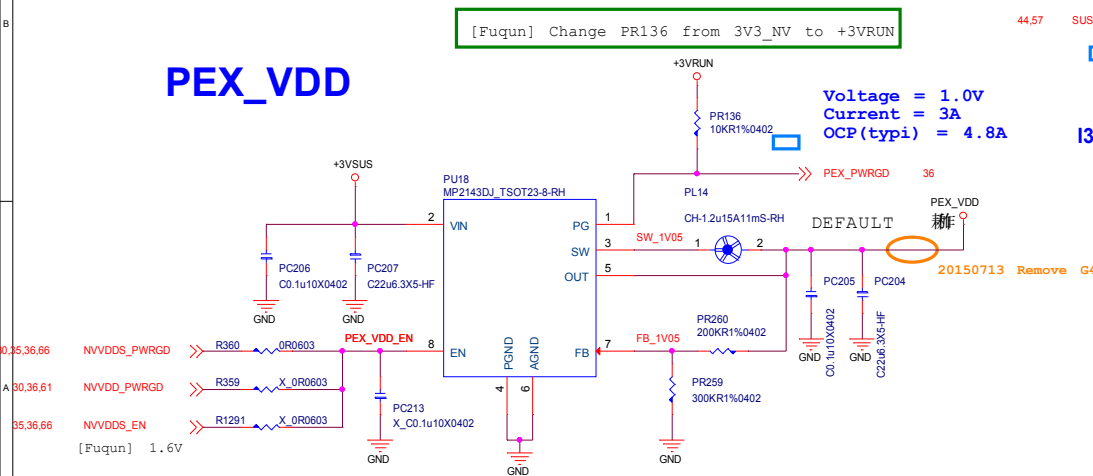
Voltage = 1.8V
Current = 0.9A

+1.2VSUS



IC MAX 3A 1A

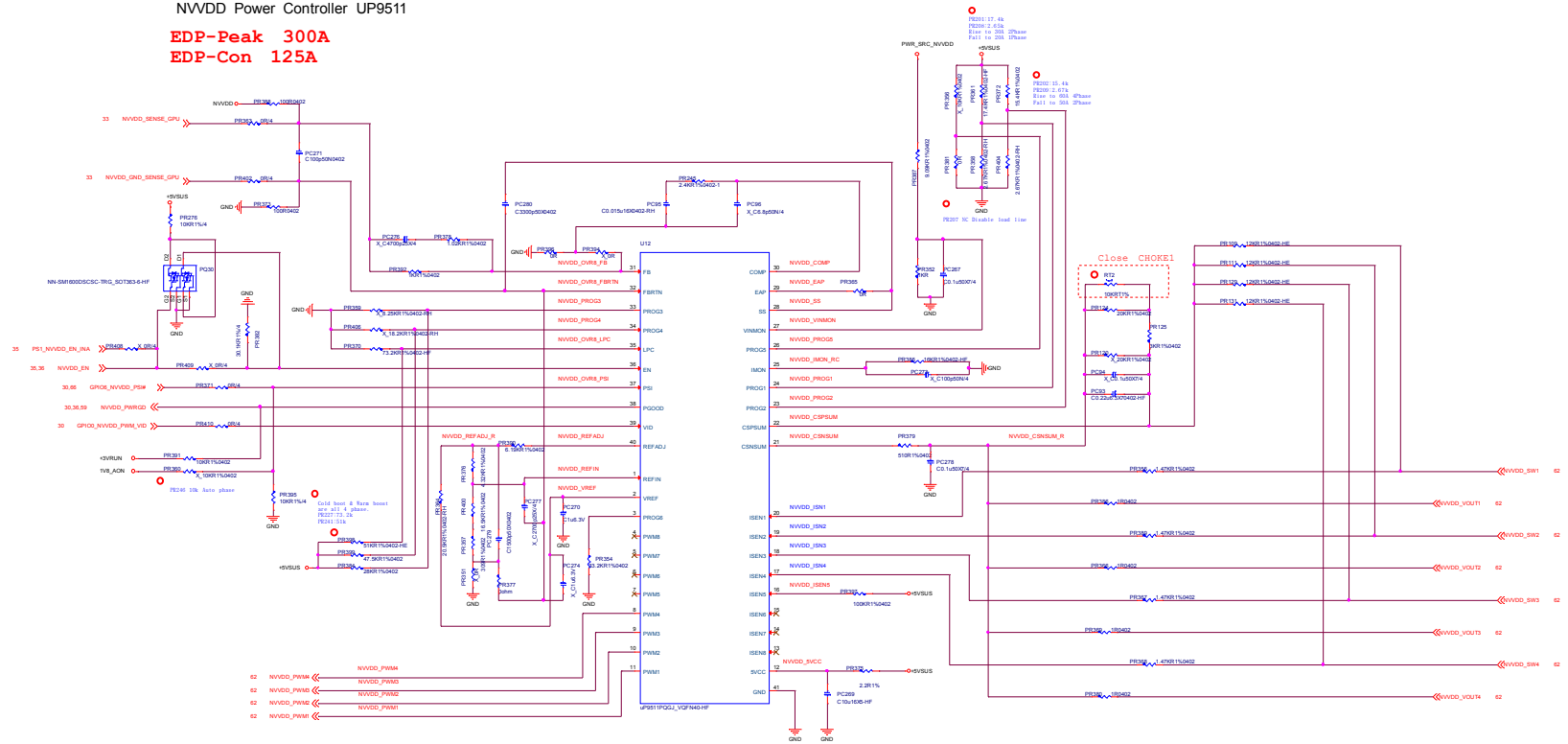
PEX_VDD



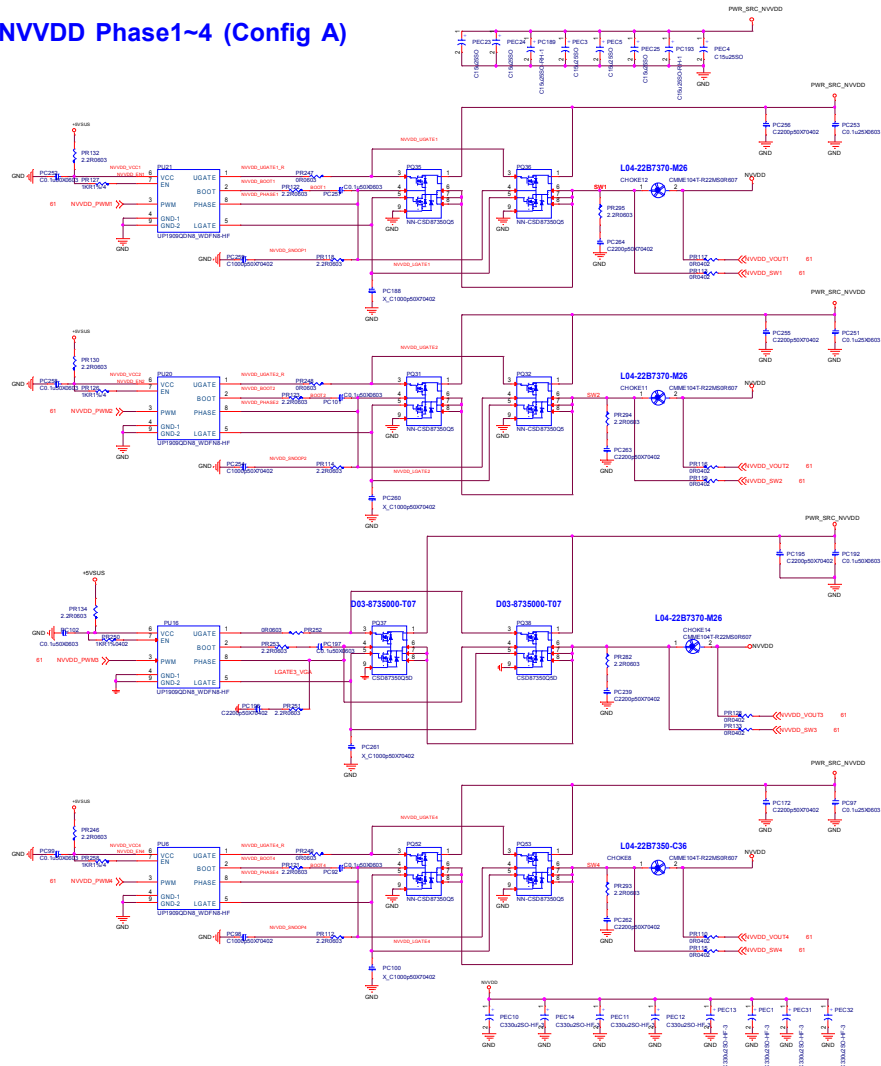
[Fuqun] Change PEX_VDD_EN from NVDDS_EN to NVDDS_PG

NVDD Power Controller UP9511

EDP-Peak 300A
EDP-Con 125A

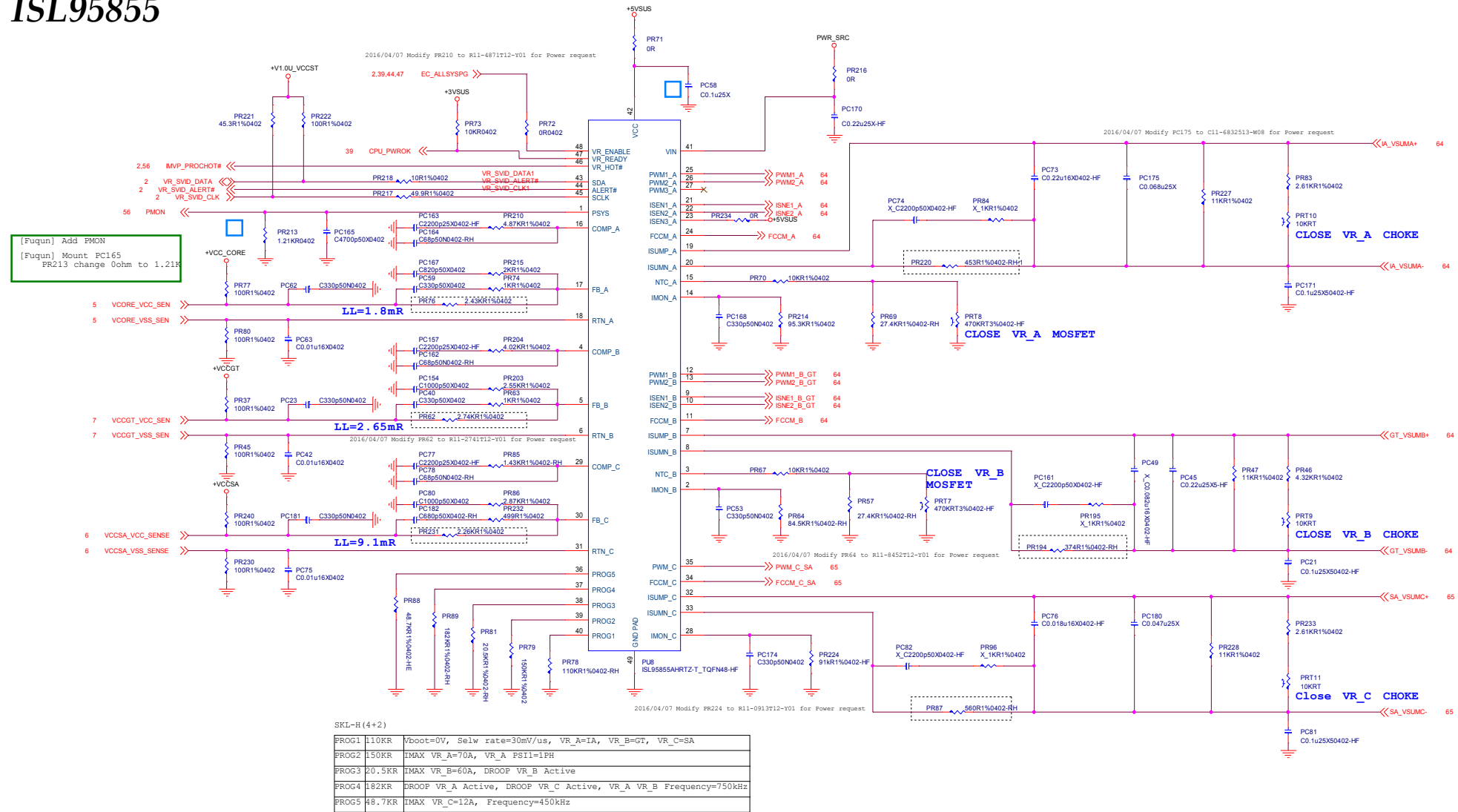


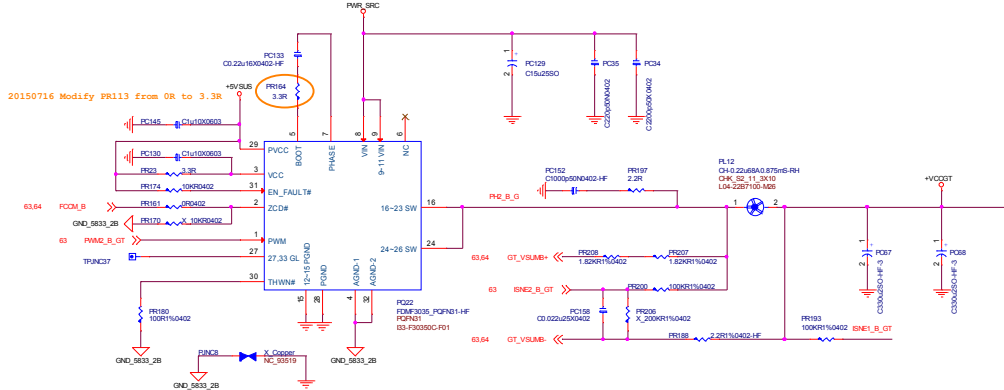
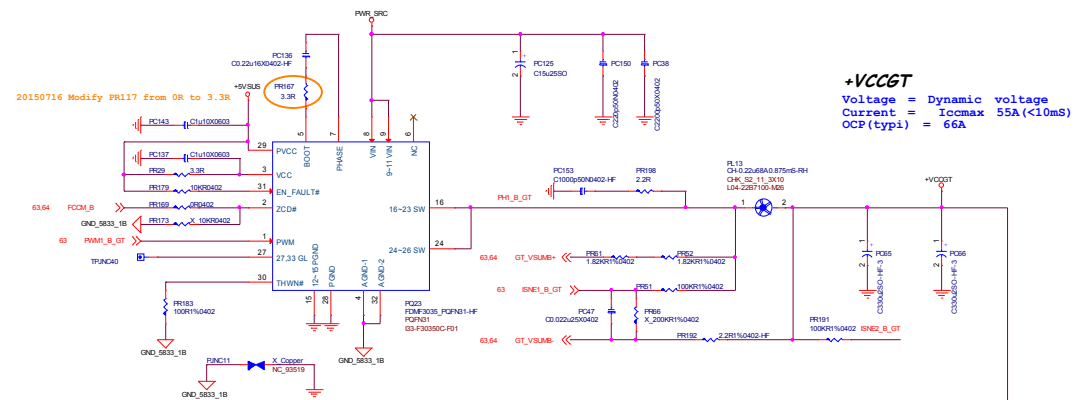
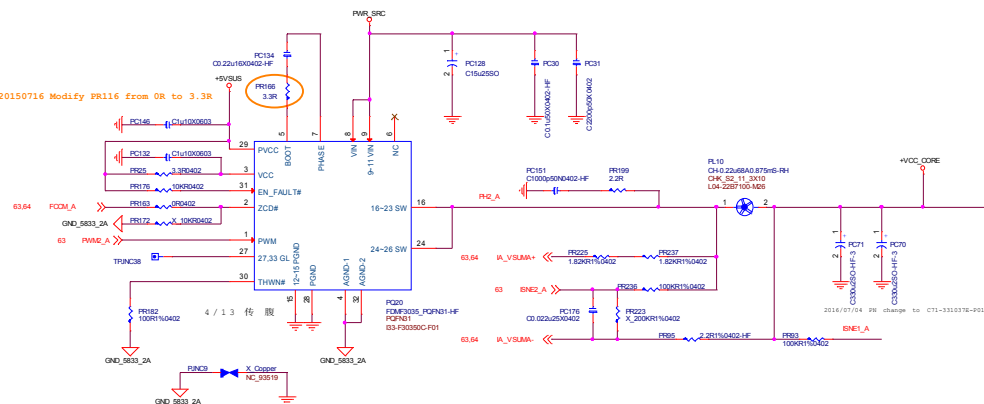
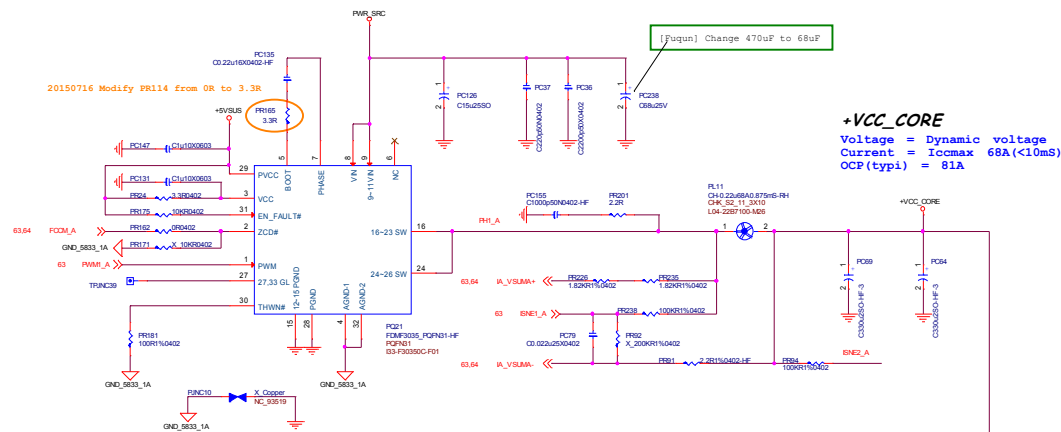
NVDD Phase1~4 (Config A)



Skylake H-line 42 45W

ISL95855





DGPU POWER / UP1666P

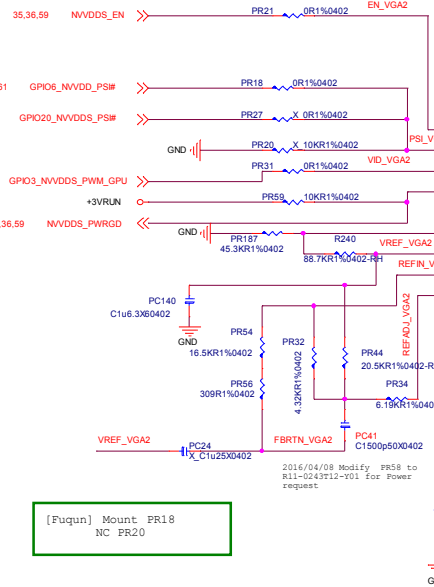
EDP-Peak 74A
EDP-Con 28A

DGPU POWER NVVDDS

VBoot:0.8V
Vmin:0.5V / Vmax:1.25V

[Fuqun] Change PR59 from 3V3_NV to +3VRUN

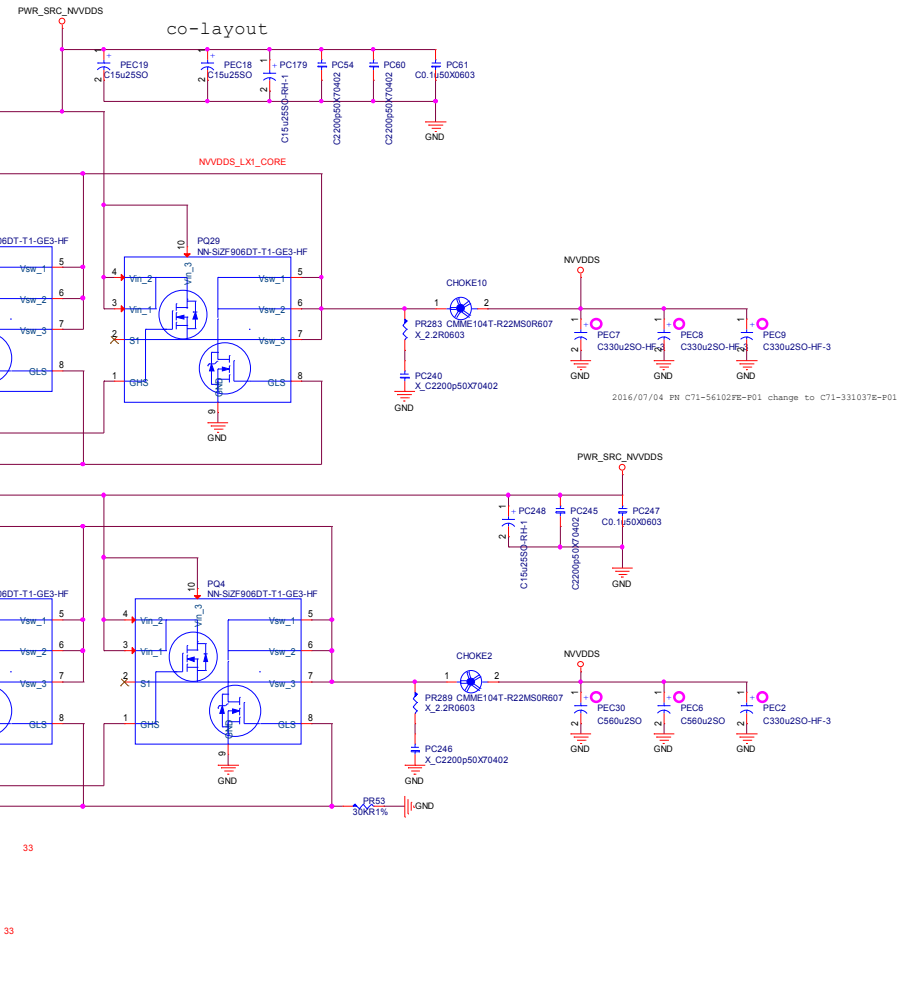
[Fuqun] 1.6V 2016/01/18 NV suggest un-stuff PR27

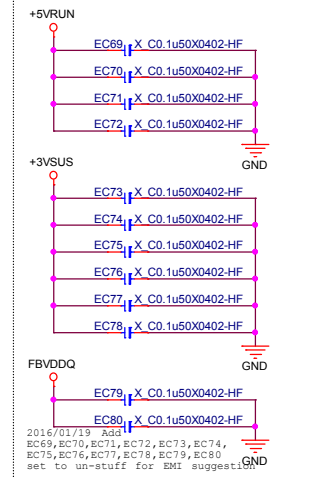
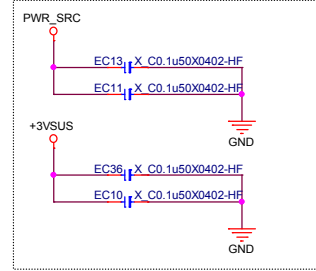
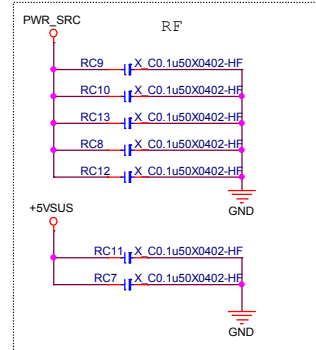
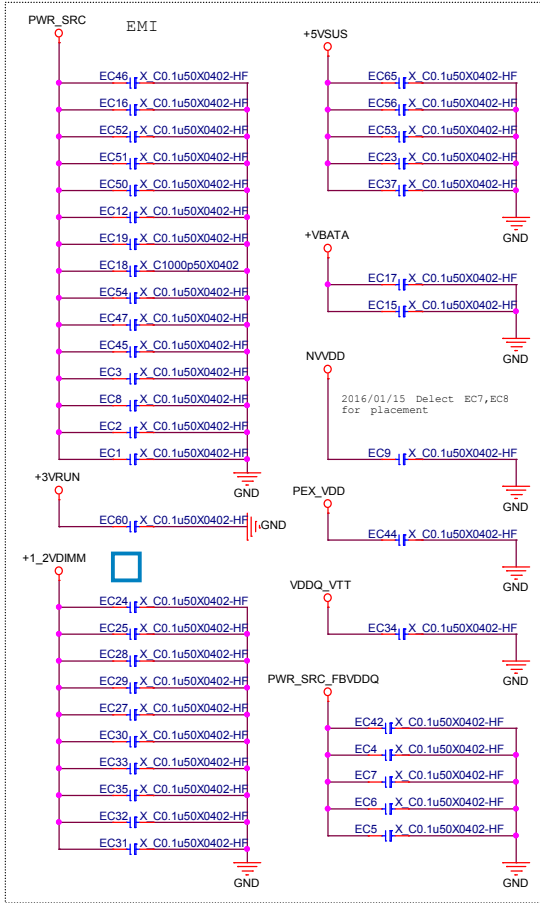


[Fuqun] Mount PR18
NC PR20

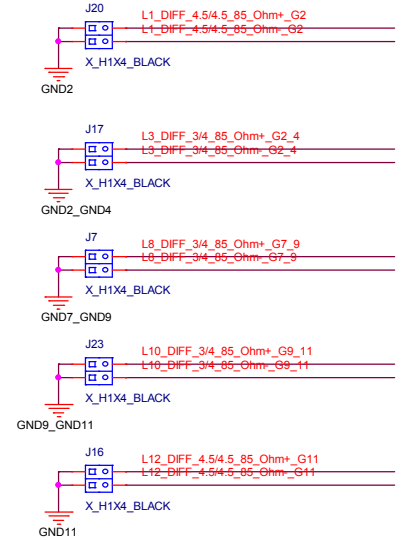
CONFIG	PR311	PR309	PR308	PR307	PR310	PC282
	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

2016/01/18 NV suggest stuff PR278, PR279

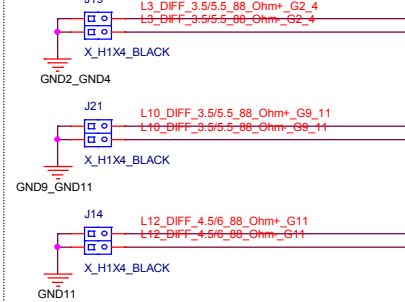




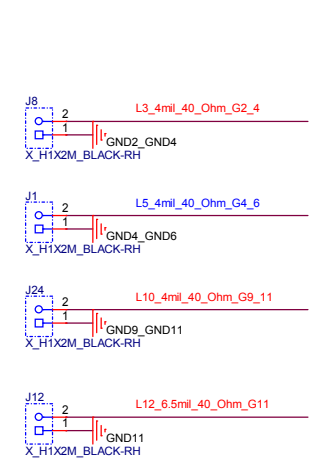
85 OHM /SATA /PCIE/ EDP /USB /DMI /HDMI /DP/CLK



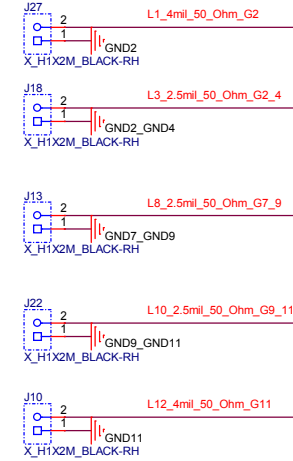
88 OHM / DDR4 DQS/CLK



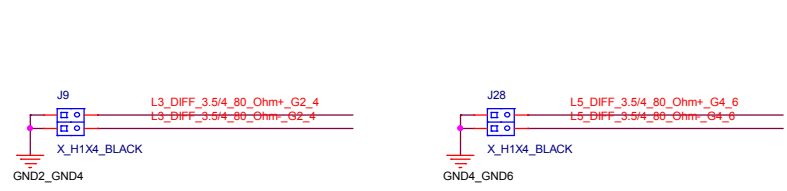
40 OHM DDR4 CMD/CTRL/CKE/ALERT



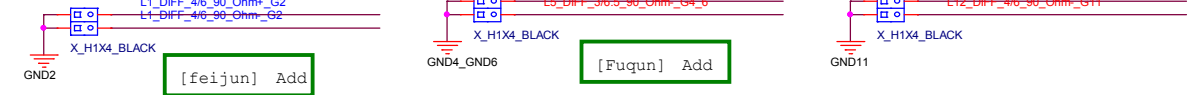
50 OHM / DDR4 DQ



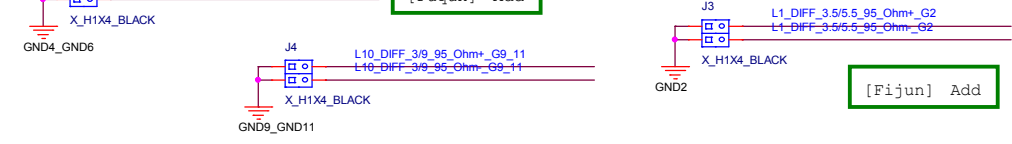
80 OHM GDDR5 CK/WCK



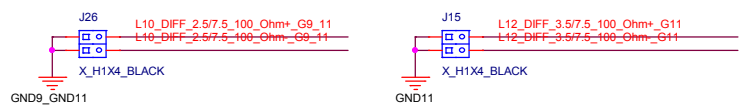
90 OHM / XTAL(GPU)

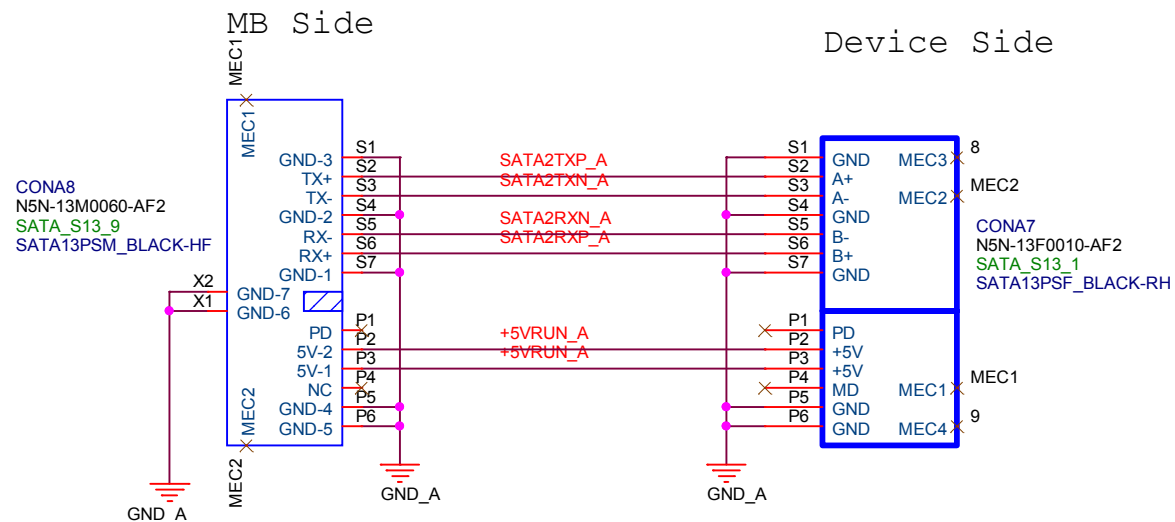


95 OHM / HDMI

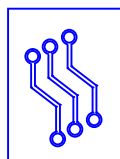


100 OHM / LAN /HDMI (After DP139)





PCBA1

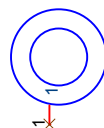


PD0-16JCA0B-H73

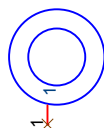
PD0-16JCA0B-H73

Hannstar: PD0-16JCA0B-H73
TRIPOD: PD0-16JCA0B-T53

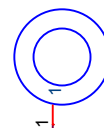
HB10
X_NPTH_80
NPTH_80



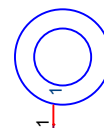
HB7
X_NPTH_80
NPTH_80



MB7
X_H_R197D91
H_R197D91_N



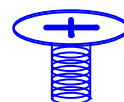
MB8
X_H_R197D91
H_R197D91_N



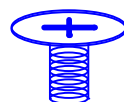
GND_A

GND_A

SCREWA2



SCREWA1



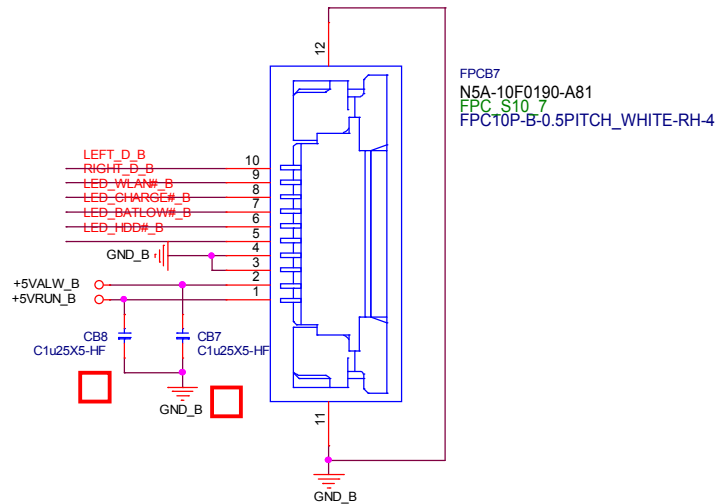
E43-1205003-H29

E43-1205003-H29

msi

MICRO-STAR INT'L CO.,LTD.

Title		
[A] 179C ODD		
Size	Document Number	Rev
A4	MS-16JC1	0B
Date:	Tuesday, October 18, 2016	Sheet 68 of 75



179C

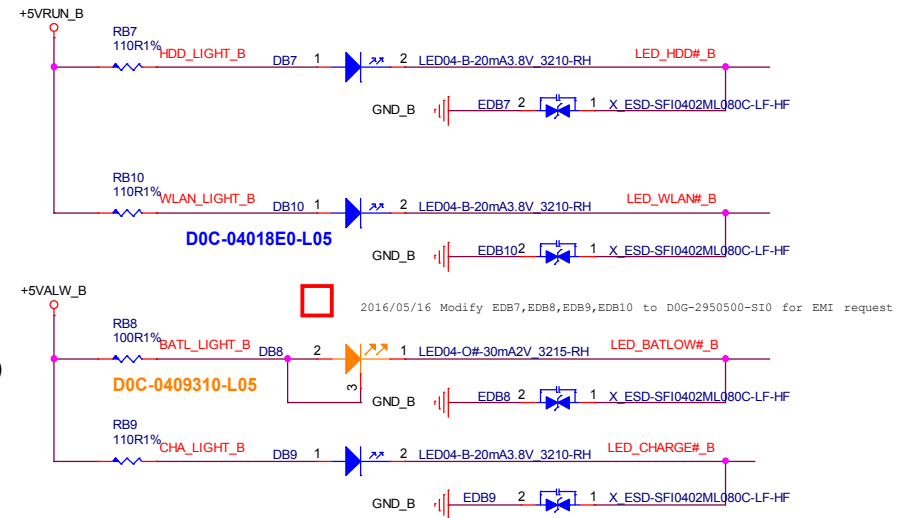
LED FRONT

BLUE
(HDD)

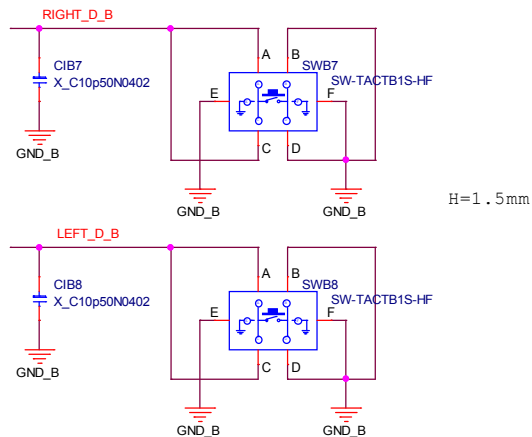
BLUE
(WLAN)

ORANGE
(BATLOW)

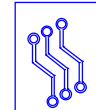
BLUE
(CHARGE)



179C

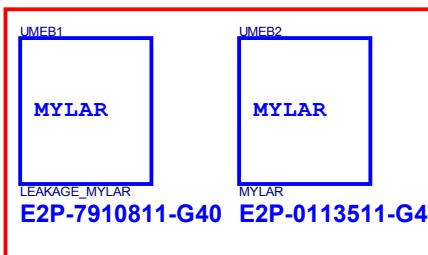
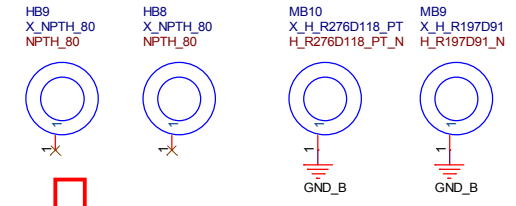


PCBB1



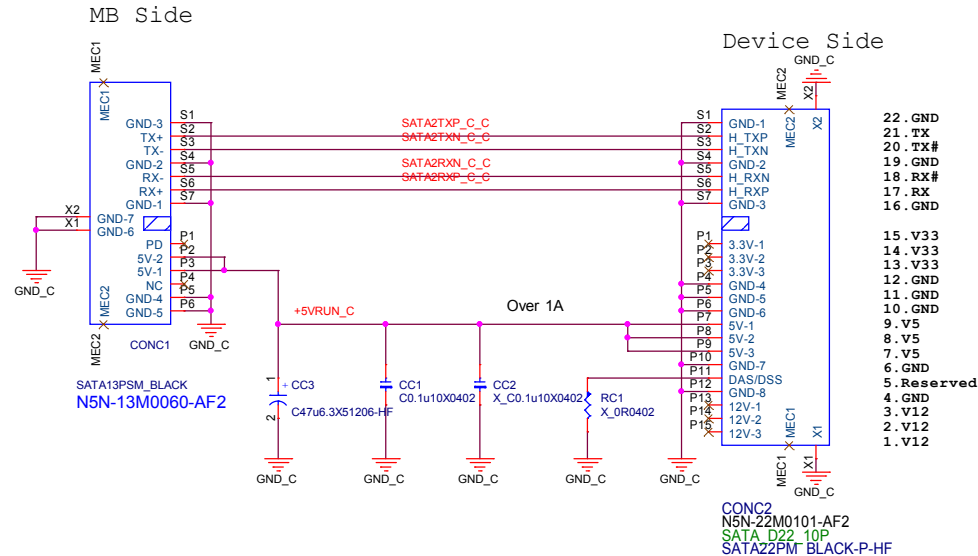
PD0-16JCB0B-H73

Hannstar: PD0-16JCB0B-H73
TRIPOD:PD0-16JCB0B-T53

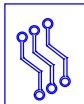


msi MICRO-STAR INT'L CO.,LTD.			
Title			
[B] 179C LED/ TP			
Size	Document	Number	Rev
B	MS-16JC1		0B
Date:	Tuesday, October 18, 2016		
	Sheet	69	of 75

Verge SATA HDD

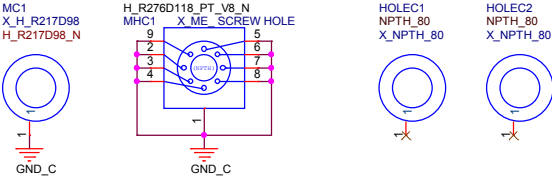


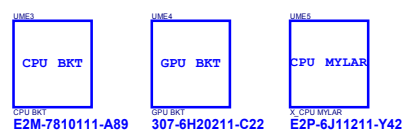
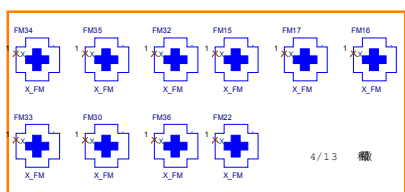
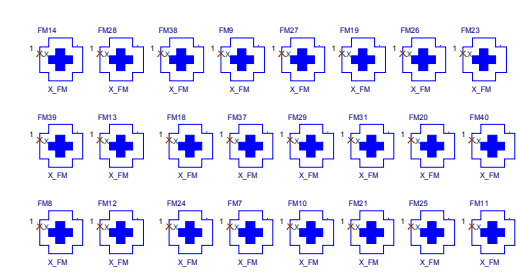
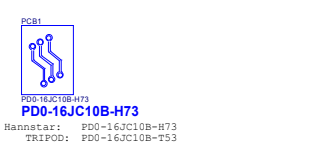
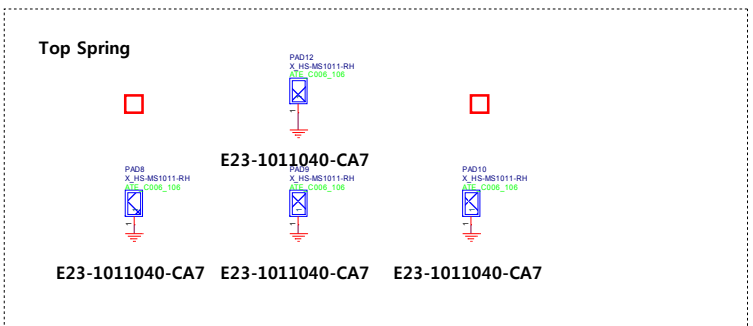
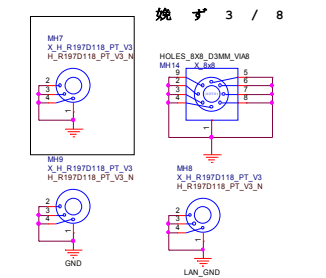
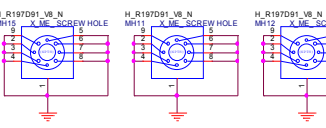
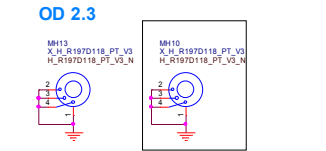
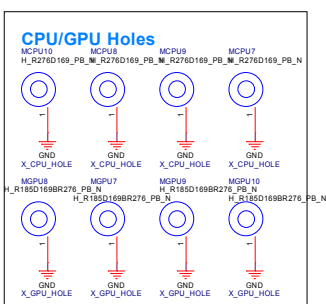
PCBC1



PD0-16JCC0B-H73
PD0-16JCC0B-H73

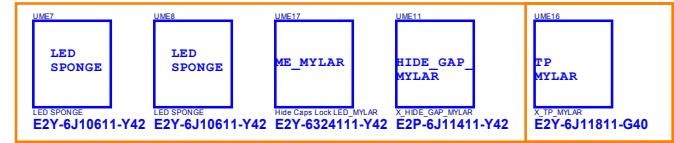
Hannstar: PD0-16JCC0B-H73
TRIPOD: PD0-16JCC0B-T53



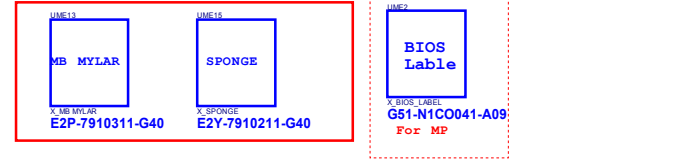


20150908 Un-staff TP mylar UME16 for ME request

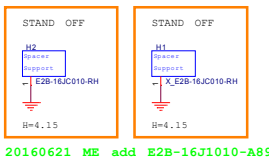
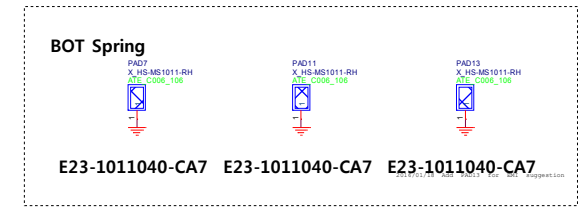
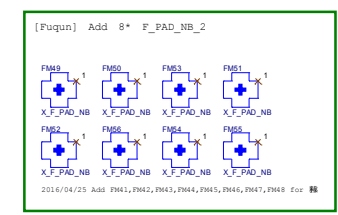
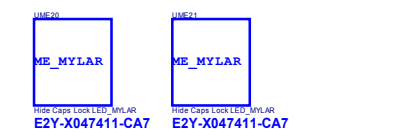
20150713 Add TP mylar UME16 for 16J4



Only 179C

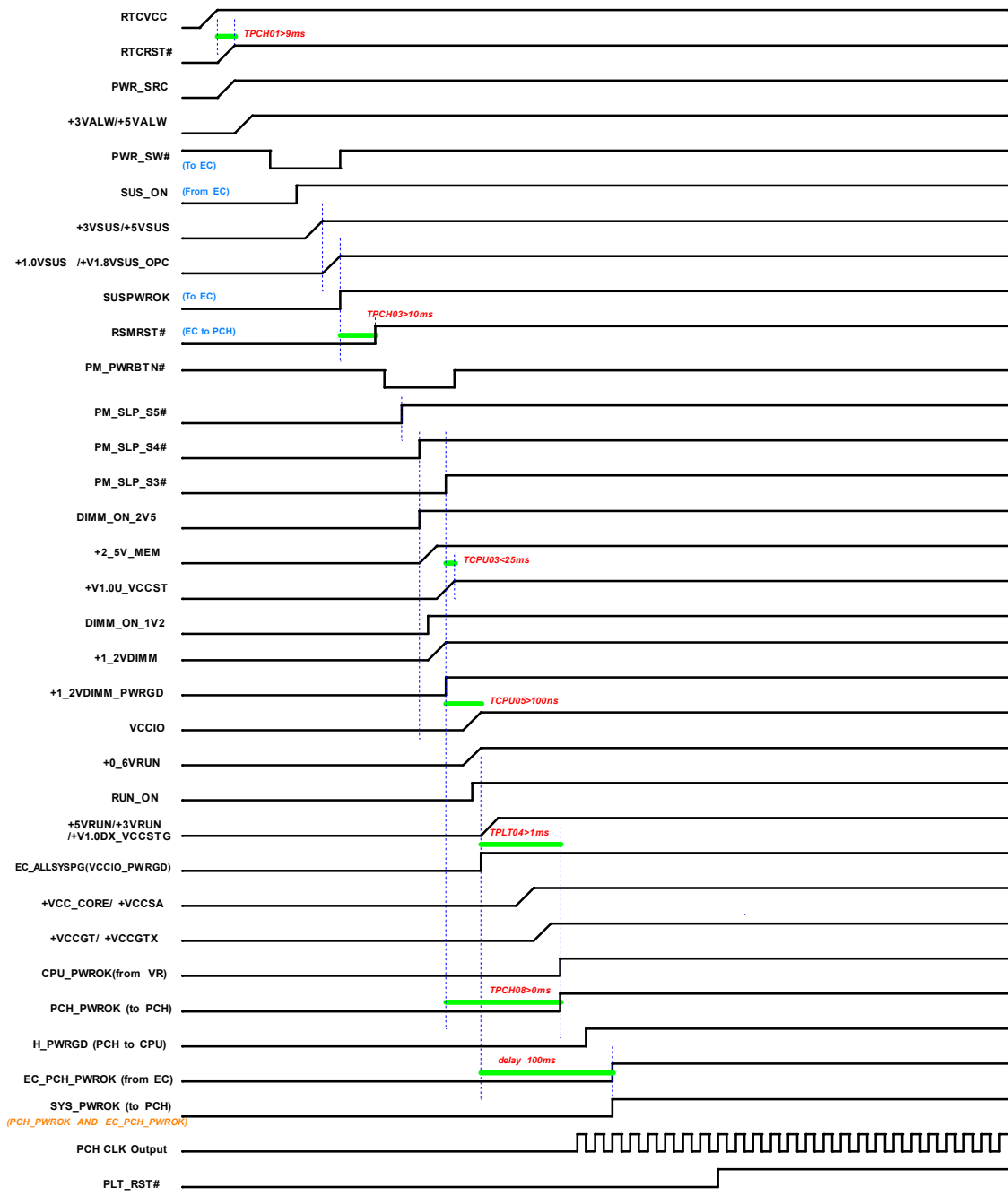


[Feijun] Add 2* E2Y-X047411-CA7 for EMI AUDIO CONT (0722)



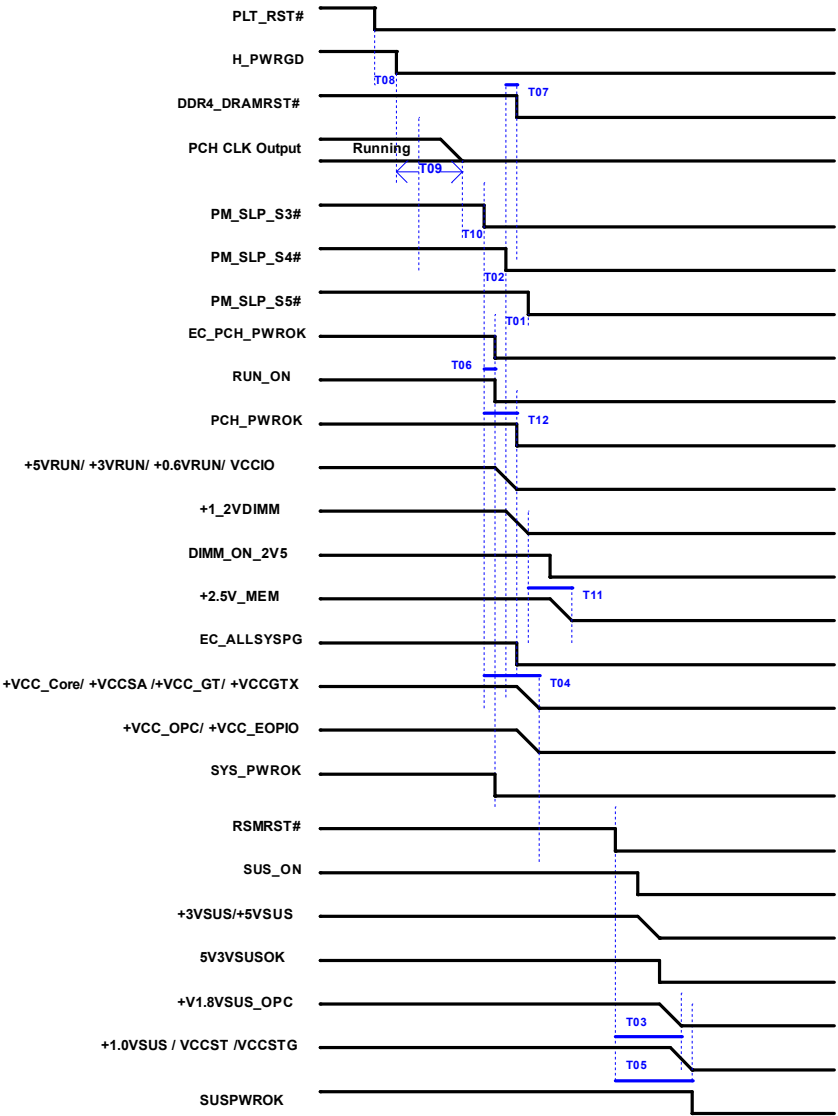
Power on Sequence

G3 -> S0



Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

History

0A		0A		10			
Page	Description	Page	Description	Page	Description	Page	Description
11	Add R3128,R3129,R3130,R3131						
18	Add R3124,R3125,R3126,R3127						
52	Remove CN7						
36	Add U76,C3318						
30	R302 stuff						
11	Remove R3128,R3129,R3130,R3131						
18	Remove R3124,R3125,R3126,R3127						
47	Add Q46,C2,R3,R5,R595,Q5						
48	Add Q50,R586,R588,R368,R364,C2839						
41	Add R478						
50	Add R3124,R3125						
67	Add H9,H10						
28	R460,R468 nostuff						
28	R115 stuff,R102 no stuff						
30	add R3126,R3127,R3128,R3129						
56	add Con13						
61	add FEC34,PEC35,PEC36,PEC37,PEC38						
25	add C3389,C3390,C3391						
56	add PL15						
61	Remove PEC36						
62	Remove PEC33						
58	add PC252						
58	add EC83,EC84,EC85,EC86,EC87,EC88,EC89,EC90,EC91						
48	Remove ER10,ER11,ER12,ER13						
62	PR20 no stuff,PR18 stuff,						
30	R302 stuff						
64	PC238 stuff						
67	Remove Footprint:F PAD NB 1 PN FM41,FM42,FM43,FM44,FM45,FM46,FM47,FM48						
67	add UME20,UME21						
70	Remove SCREW C1.SCREW C2						
39	c547,c580 2.2uF change to 10uF(C11-1067312-M09)						
49	add R1293,R1294						
25	Remove C281,C282,C244,C245,C383,C384,C362,C363						
71	H7,H8,MB7,MB8,MB9,MB10,M C1,MCPU7,MCPU8,MCPU9,MCPU10, MGPU7,MGPU8,MGPU9,MGPU10,MH7,MH8,MH9,MH10,MH11,MH12, MH13,MH15,MH C1 footprint change add _N						
48	ADD L17						

